User Hardware Handbook

CENTRAL PROCESSOR UNIT
CONTROLS AND MONITORING

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CPU CONTROLS AND MONITORING

CONTENTS

TABLES

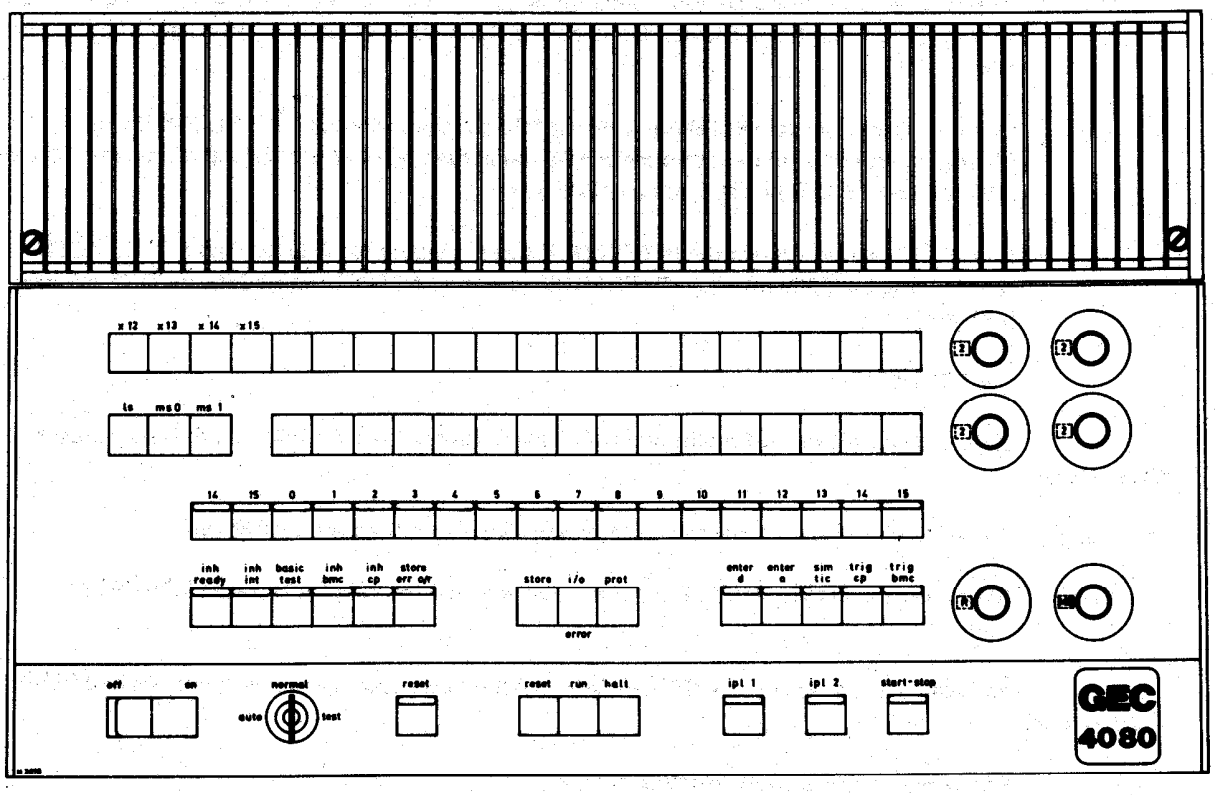
1 INTRODUCTION

The Control and Monitoring Unit (CMU) comprises the lower half of the CPU front panel assembly, and consists of control switches and indication lamps mounted, with their associated circuitry, on a printed circuit board at the rear of the front panel.

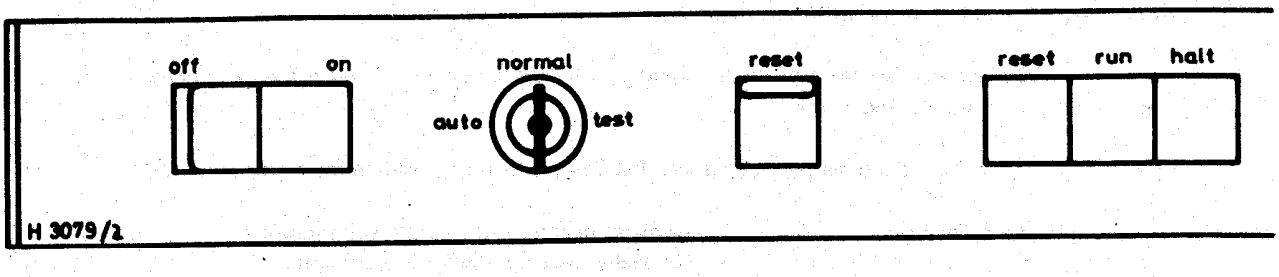
Connections are taken from the board by a lighweight cable to three top edge connectors on the Control Monitor card in the logic rack.

The controls and lamps are split into five rows; which are, reading from bottom to top.

(a)	Basic Controls:-	Controls necessary to operate the equipment Normally used for ON/OFF operation.
(b)	Engineers Controls:-	Used for Commissioning or maintenance purposes.
(c)	20 Data Keys (18:4080):-	Data source for program including IPL, and manual tests.
(d)	19 Data Highway Monitor Lamps:-	Display data words on highways selected by rotary switches DA and DB
(e)	20 Address Highway Monitor Lamps:-	Display address words on highways selected by rotary switches AA and AB.



4080 CMU PANEL



2.1 ON/OFF

The ON/OFF switch is a rocker switch which controls the mains supply to the unit. If switched to the ON position, AC mains is provided via a cable at the rear of the unit to a MAINS DISTRIBUTION UNIT (MDU) where a relay is energised to switch mains supply to the Power Supply Unit of the CPU and to other units (stores, peripherals, etc.) in the system. If switched to the OFF position, AC mains is removed from the MDU which in turn opens the relay to remove mains from the CPU and other units powered from it.

NOTE One side of the mains switch remains alive.

Switch ON

When the CPU is switched on by the application of mains supply to the PSU, the following sequence takes place:-

(a) When DC rails in the CPU are established correctly the machine will be placed in the RESET state with the HALT and RESET lamps illuminated, STORE ACTIVE and ACTIVE signals will be held false.

(b) When the Rails Correct (RC) signal from the PSU becomes true and INTERLOCK is true (indicating that other units within the configuration have powered-up correctly) then after 200 ms ACTIVE and STORE ACTIVE will be made true.

(c) If when DC rails are correct the INTERLOCK signal is false, then ACTIVE and STORE ACTIVE remain false until 200 ms after INTERLOCK goes true. ACTIVE and STORE ACTIVE are then both made true.

Switch OFF

If the CPU is switched off by the removal of mains supply from the PSU, the following sequence takes place:-

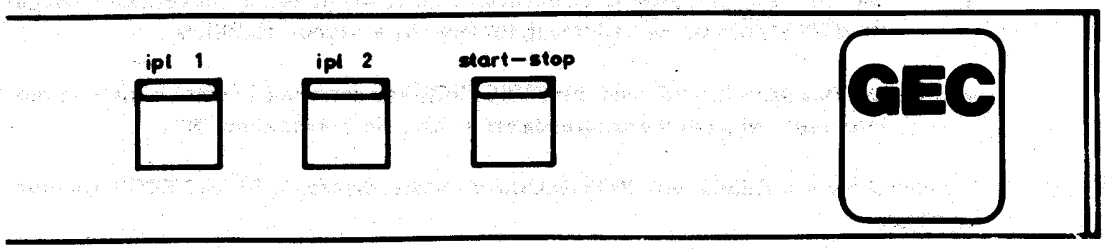
(a) The ACTIVE signal is taken false and a 'Power Fail' Error interrupt is generated.

(b) After 1 ms the STORE ACTIVE signal is made false and the machine is placed in the RESET state.

The same actions occur if the INTERLOCK signal is taken false, indicating Power Failure elsewhere in the system.

For further details see CPU Nucleus manual.

Escutcheon marked 4070
4080 or 4082 - as appropriate.



2.2 PANEL MODE SWITCH

Adjacent to the ON/OFF switch is a 3-position key operated switch enabling the panel to be used in one of three modes.

(a) *Normal*

The basic controls and Data Keys are operative.

(b) *Test*

All controls are operative.

(c) *Auto*

The ON/OFF control only is operative. Switch-on causes an automatic program start by placing the machine in the RUN state. No Initial Program Load (IPL) sequence is possible.

2.3 RESET, RUN AND HALT LAMPS AND SWITCHES

Reset

The RESET lamp is illuminated if the machine is halted (with the HALT lamp illuminated) and is in its quiescent reset state.

If the machine is not in the RUN state (e.g. the RUN lamp is extinguished) it may be placed in the RESET state by depressing the RESET key. This has the effect of

(a) Placing the clock in its reset state if it was stopped by a 'Busy' condition.

(b) Resetting interfaces by taking the ACTIVE and STORE ACTIVE interface lines false for at least 200 ms.

(c) Resetting the internal logic of the CPU and BMC.

Start/Stop

The RUN lamp is illuminated if the internal clock of the machine is running; whilst the HALT lamp is illuminated if the clock is stopped in its reset state. If the HALT lamp is illuminated and the RESET lamp is extinguished the machine is in the HALT state.

(a) If the START/STOP key is depressed whilst the machine is in the RUN state the CPU/BMC is put into the HALT state at the end of the current CPU instruction or BMC cycle. Depressing the START/STOP key whilst the machine is in the HALT state causes operation to be resumed with the next-instruction in sequence and/or the next BMC cycle in sequence.

(b) If the START/STOP key is depressed whilst the machine is in the RESET state the machine is put into the RUN state and one of the following initial start sequences is performed:-

(i) with the panel in NORMAL or the BASIC TEST key up (i.e. in full nucleus mode) a 'load HSR' operation is performed, followed by a nucleus reschedule.

(ii) with the panel in TEST and the BASIC TEST key depressed an entry is made to the interrupt level, with the cause code set to 13_{10} (in store location 0)

NOTE If the machine is in RESET with INTERLOCK held false, depressing START/STOP will have no effect.

Operation in Auto

If the CMU is switched to AUTO mode the START/STOP and RESET keys are inoperative. The machine is placed in the RESET state after switch on (as described in 2.1.1.) or after power failure (as described in 2.1.2.). After ACTIVE and STORE ACTIVE have been made true, an automatic START signal is generated by the processor, which has the same effect as depressing the START key with the machine in RESET.

If the machine is in AUTO, it can only be halted by switching its mains power off, or by breaking the INTERLOCK signal to the CPU (see 2.1.b)

2.4 IPL

The Initial Program Load facility of the processor provides a method of loading software into an empty machine, and triggering its execution.

The facility is performed by copying a short 'Initial Input' program, into store, from ROMs mounted on exchangable IPL Assemblies (IPLAs). The initial input program is then actioned to load software into store from a selected input device.

Two IPLAs may be fitted to provide a choice of IPL from alternative types of device. The IPLAs are easily exchanged, allowing the selection of input device to be varied.

IPL Sequence

The IPL sequence is initiated by depressing either of the IPL keys (IPL1 or IPL2) on the CMU panel. For this to be effective:-

(a) The CMU must be in the RESET state (HALT and RESET lamps lit).

(b) The CMU panel must be in NORMAL or TEST.

If both of the above conditions exist the sequence is as follows:-

(i) The processor is forced into BASIC TEST mode, regardless of the state of the BASIC TEST key on the front panel.

(ii) An Initial Input Program is copied into Store locations 0 upwards, from IPLAs. One of two possible programs is loaded depending on whether IPL1 or IPL2 is selected.

(iii) The Initial Input program is now triggered at interrupt level such that the contents of locations 22 and 24 in Store are loaded into the Sequence Register and Local Register respectively.

(iv) The Initial input program is now executed, and will normally read program and data from an appropriate input device, triggering the system it has loaded.

2.5 IPLAs

The ROMs containing the Initial Input programare on two IPLAs, mounted on the top edge (EC5 and EC6) of the Arithmetic board of the CPU. Each IPLA provides up to 128 bytes of Initial Input program. In the following pages the IPLA on EC5 will be called Assembly A and that on EC6, Assembly B.

If key IPL1 is depressed, the content of Assembly A is loaded into bytes 0-127 of Store, the other locations in store being unchanged; whereas if key IPL2 is depressed, the content of Assembly B is loaded into bytes 0-127 of Store and the content of Assembly A is loaded into bytes 128-255.

2.6 USAGE

Loading of the IPLAs by use of keys IPL1 and IPL2 may be executed in three ways.

(a) With only one IPLA fitted (Assembly A on EC5) IPL1 is always used and IPL is available only from one device.

(b) With both IPLAs fitted independant Initial Input programs from two different devices can be held. IPL1 and IPL2 can then be used to select which Initial Input program (A or B) is to be used.

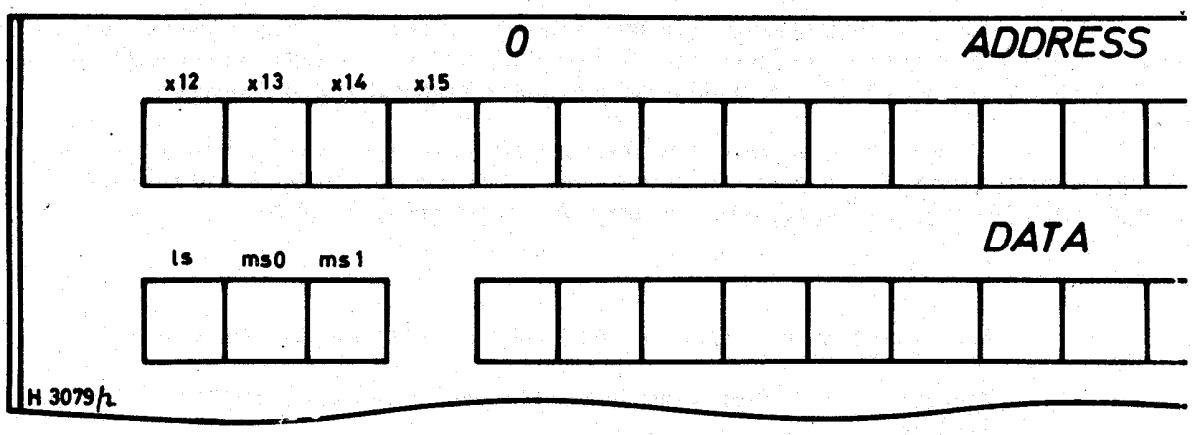
(c) With both IPLAs fitted they can be employed to hold a single program for a more complex device. In this instance key IPL2 must always be used to load both IPLAs.

Loading of Full Nucleus Systems

Operation of either of the IPL keys forces the machine into Basic Test mode. When loading of the full Nucleus system is completed, it is necessary to switch the machine to full nucleus mode to commence execution. The two methods of achieving this are:-

(a) Stop the machine at completion of loading , by operation of the START/STOP key or by a HRK instruction. Ensure that the BASIC TEST key is in the up position, or that the CMU is in NORMAL mode.
Press the RESET key to assert the Full Nucleus mode, and then press the START/STOP key to start the machine running. A Nucleus reschedule operation will be performed and system software will be entered.

(b) By obeying a SFN (Set Full Nucleus) instruction. This sets Full Nucleus Mode, provided that the BASIC TEST key is in the up position or that the CMU is in NORMAL, thus causing a Nucleus reschedule to enter the Full Nucleus system.



3.1 GENERAL

The three rows of monitoring lamps and data keys are aligned so that the corresponding bits are directly beneath one another.

The data keys (Figure on pages 8 and 9) have four functions:-

(a) As a source of data for input to the data registers. Keys labelled 0-15 provide the 16 data bits. The keydata is routed onto the appropriate data highway via the data lines from store.

(b) As a source of data for input to address register, enabling all stores to be directly addressed - in half words. Keys are labelled as follows:

4080: X14, X15, 0-15 provides a full 18 bit addressing,
4070: X13,X14, X15, 0-15 provides a full 19 bit addressing,
4082: X12, X13,X14, X15, 0-15 provides a full 20 bit addressing.

(c) As a source of data used as a standard to compare with address selected data (see Usage of Engineers Controls).

(d) As a source of data for the RK (Read Keys) and HRK (Halt and Read Keys) instructions. If the machine is in Auto, the Data Switches act as a source of zeros.

There are 20 Address Monitoring Lamps designated x12 - x15, 0 - 15. The 20 bits are necessary to display base and range registers simultaneously.

The 19 Data Monitoring Lamps are split into 2 groups:-

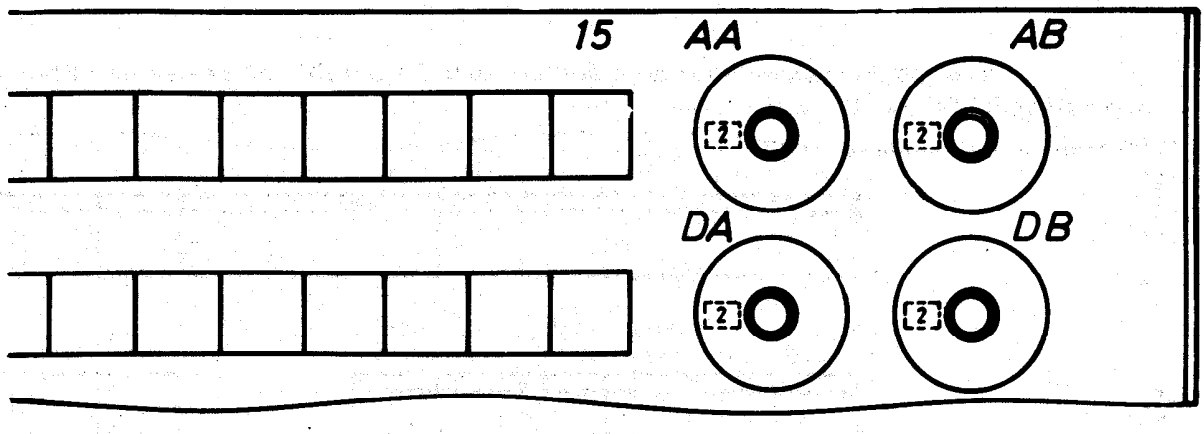
(a) Labelled 0 - 15 for 16 bit and other data registers.

(b) Labelled ls , ms0 and ms1 for information on register end effects (shifts, carries, etc.).

3.2 METHOD OF MONITORING

A large number of points are monitored by the built-in facilities enabling fault diagnosis to be made fairly accurately.

Most boards may place data/control waveforms onto either or both of two monitoring highways with the lamps directly displaying their logic state.



Data to be placed on a highway is selected by two 8-way switches mounted beside each row of monitoring lamps enabling up to 64 words to be monitored.

Address Highway Monitoring

The highway is 20 bits wide and monitors address registers and control waveforms. For details see Tables 1-10.

Data Highway Monitoring

The highway is 19 bits wide and monitors data registers and control waveforms. For details see Tables 1-10.

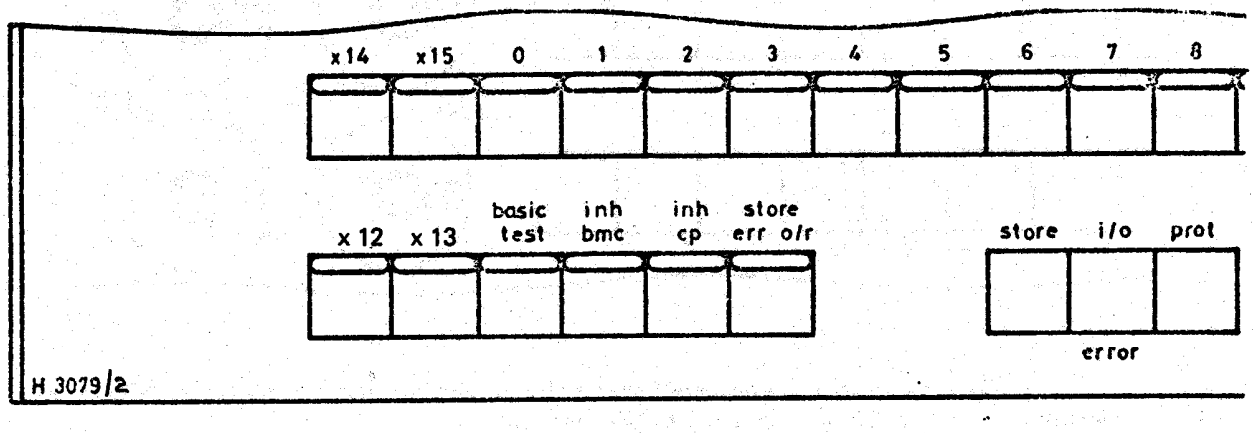
Monitoring in RUN State

Tables 1-10 list the Register and Control waveforms when the machine is in the HALT state.

When the machine is in the RUN state the following registers cannot be monitored as they share highways. Setting the switches to one of these registers selects the appropriate common highway.

AL,AM, BL, BM L, S, X, Y, Z W_1, W_2, W_3	Data monitor highway switch setting 50 (main Reg.) selects common highway for these registers.
Q_{1-4}	Data selection switch setting = 51 selects common Q reg. highway
U_{1-4}	Data selection switch setting = 62 selects common U reg. highway.

The annotations shown are related to 4070 and 4082. On the 4080 x 12 is marked INH.READY and x 13 is INH. INT. refer to Figure on page 1.



A comprehensive set of controls are provided. These are described individually in this Section. Their usage is described in Section 5. As mounted on the front panel they form a row beneath the data keys.

4.1 CONTROL KEYS

A group of 6 keys on the lefthand side of the panel inhibit certain facilities for test purposes. They are only active in the test mode.

INHIBIT READY (4080 only)

A locking control that in the down position prevents the BMC from servicing any external readies.

INHIBIT INTERRUPT (4080 only)

A locking control that in the down position inhibits all interrupts from the BMC and Command Interface.

BASIC TEST

A locking control that in the down position locks out the segmentation feature and replaces the other nucleus features with a few simple I/O instructions. The BASIC TEST switch is depressed when certain simple test programs are to be run.

INHIBIT BMC

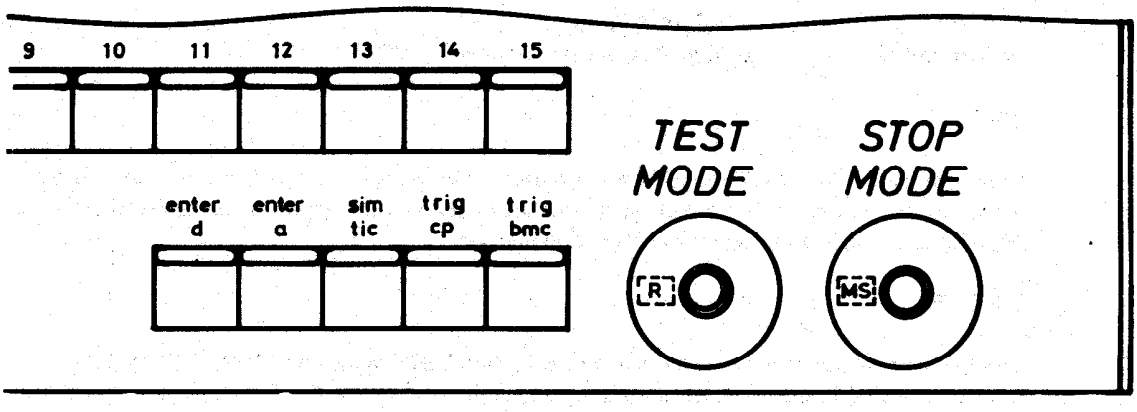
A locking control which in the down position prevents the BMC from operating by inhibiting all BMC Clocks.

INHIBIT CPU

A locking control which in the down position prevents the central processor from operating by inhibiting all CPU clocks.

STORE ERR O/R

A locking control which in the down position prevents the CPU or BMC from taking any action on time out or parity errors.



4.2 ERROR LAMPS

A group of 3 lamps that indicate an error has occurred. They are lit independently of any action the CPU or BMC may take.

STORE ERROR

The lamp is lit whenever a store parity or timeout error occurs giving a visual record of failure. It is extinguished by placing the machine in the HALT state.

I/O ERROR

The lamp is lit when the BMC has detected an error. It is extinguished by placing the machine in the HALT state.

PROT. ERROR

If the CPU attempts to address store in violation of the hardware protection circuitry the lamp will be lit. It is extinguished by placing the machine in the HALT state.

4.3 MANUAL TEST KEYS

A group of 5 keys mounted to the right of the error indicator lamps. These are all non-locking and only operate in the test mode.

ENTER D

The key is only operative when the machine is in the HALT, state. When depressed data (bits 0-15 from the data keys) is entered into a register selected by the data selection switches. The following registers may be loaded

Am, Al, Bm, Bl, S, L, X, Y, Z
W1, W2, W3
Q1, Q2, Q3, Q4
U1, U2, U3, U4

ENTER A

The key is only operative when the machine is in the HALT state. When depressed data (bits X14, X15, 0-15) from the data keys is entered into an address register selected by the address selection switches.

The following registers may be loaded:

IA	- Instruction Register
VA	- Virtual Store Address
ROMAD	- R.O.M. Address
BMC ROMAD	- Basic Multiplexer Channel R.O.M. Address

SIMTIC

Only operative in the HALT state. When depressed it clocks data into the F and G latches at the output of the arithmetic unit. When stepping through the microprogram it may be used for checking data routing through the shifter to the register.

TRIG CP

This key is only operative when the machine is in the RESET state, and BASIC TEST mode is selected. the CPU enters the RUN state and actions the next instruction in sequence if the TRIG CP switch is held down whilst the START/STOP key is depressed.

In all other circumstances the TRIG CP key has no effect.

TRIG B.M.C.

When depressed it causes the CPU to simulate a direct output to the BMC. For details of usage see Section 5. The key is not operative when the CPU is in the RESET state.

4.4 TEST AND STOP MODE SWITCHES

STOP MODE SWITCH

The 8-position switch controls the operation of the clock. The switch should only be operated when the machine is in the HALT state.

ABBREVIATION	POSITION	FUNCTION
0	1	OFF This position allows continuous operation of the clock, which can only be stopped by operation of the START/STOP key.
IS	2	INST. STEP The clock is stopped (placed in HALT state) at the end of an instruction (or BMC transfer) With the machine in the HALT state every depression of the START/STOP key will cause an instruction and/or BMC transfer cycle to be obeyed.
MS	3	MICROSTEP With the machine in the HALT state every depression of the START/STOP key causes the CPU and/or BMC to execute one step of the microprogram (see NOTE)
IO	4	I/O ERROR STOP If the BMC detects an I/O error the clock is stopped at the microstep and the I/O ERROR and HALT lamps light.

ABBREVIATION	POSITION	FUNCTION
ST	5	STORE ERROR STOP The clock is stopped and HALT lamp lit if a store parity or timeout error is detected. On restart, by depressing START/STOP the machine branches to error routine. If the ERROR override key is down the machine may be restarted in the normal way.
SN	6	SYNC. STOP The clock is stopped and HALT lamp lit if the data in a pre-selected register is identical with the setting of the data keys. The data to be compared is determined by the setting of the address selection switches The facility is available for SA - Store address 23 VA - Store virtual address 21 BMC SA - BMC store 70 IA - CPU Instruction Register 41 ROMAD - ROM Address Register 27 BMC ROMAD - BMC ROM Address 71
	7	Position Not Used

NOTE The microstep mode is normally used with either BMC or CPU operation inhibited.

4.5 TEST MODE SWITCH

An 8 position switch providing test facilities. Positions 2-6 enable data to be read from, or written into, store using the BMC. All CPU clocks and I/O transfers are inhibited.

Positions 7 & 8 are used for CPU tests.

The switch must only be operated when in the HALT state.

The TEST MODE SWITCH is used in conjunction with the STOP MODE SWITCH to enable single shot or continuous operation.

ABBREVIATION	POSITION	FUNCTION
0	1	OFF Position
EA	2	ENTER ADD On depressing START/STOP data from the data keys (x14, x15, 0–14) is transferred to the BMC to be used as an 18 - bit store address, the least significant bit being zero.
R	3	READ On depressing START/STOP the BMC reads a half-word from store into the input/output register addressed by the BMC store address register, plus: X13 for 4070 or X12 and X13 for 4082. This can be monitored by the data highway monitor (setting 07). The address would normally have been previously set by using the ENTER ADD facility.
W	4	WRITE On depressing START/STOP the BMC writes into store data from the keys (0-15) into a location addressed by the BMC store address register,plus: X13 for 4070 or X12 and X13 for 4082.
RI	5	READ INCREMENT As for position 3 only the BMC Store Address register is incremented by 2 (1 halfword address) after each operation.
WI	6	WRITE INCREMENT As for position 4 only the BMC Store Address register is incremented by 2 (1 halfword address) after each operation.
01	7	OBEY 1 The IA register, which holds the next instruction to be obeyed, is prevented from being loaded from store. Hence an instruction may be continuously obeyed. Store operands are taken from data keys (0-15)
02	8	OBEY 2 As OBEY 1 only with operands from store.

5 USAGE OF CONTROLS

The basic controls, START/STOP and RESET are used in normal operation and with the engineering controls.

5.1 BASIC CONTROLS ONLY

(1) STARTING

Switch on with key operated mode switch not in AUTO. If in TEST check that both STOP MODE and TEST MODE switches are in the OFF position. Machine is in RESET and HALT.

Depress START/STOP only if basic software and systems tables are in store. Otherwise depress one of the two IPL keys. The machine will remain in RUN state unless an HRK instruction is obeyed.

(2) STOPPING

Depress START/STOP key. CPU and BMC will complete their current instructions before the clock is stopped. Autonomous transfers may not be completed correctly dependent on peripheral type.

(3) RESTARTING

(a) If a restart is required from the same place as the machine was stopped then depress START/STOP key.

(b) If a new start is required depress RESET key and release followed by START/STOP key. If in full Nucleus a load of HSR and reschedule is performed. (see 2.3)

5.2 BASIC CONTROLS WITH ENGINEERS CONTROLS

The controls may be used in many combinations. The Section gives some of the more common examples:-

(a) *To Monitor a Data Register*

Stop the clock if in RUN by depressing START/STOP key. Set up the required address on the data switches. For full details see Tables 1 - 10.

(b) *To Monitor an Address Register*

Stop the clock if in RUN by depressing START/STOP key. Set address highway selection switches as follows:-

Common examples -	VA	21
	IA	41
	BMC SA	70

For full details see Tables 1 - 10

(c) *Loading a Data Register*

(1) Stop clock if in RUN by depressing START/STOP key

(2) Select register on data selection switches

(3) Set up data on data keys 0-15

(4) Depress ENTER D key

(d) *Loading an Address Register*

(1) Stop Clock if in RUN by depressing START/STOP key
(2) Select register on address selection switches
(3) Set up address on data keys
(4) Depress ENTER A key instruction

The monitoring and loading of registers is independent of microprogram and may be carried out at any time, e.g. while micro-stepping through an instruction.

(e) *Loading Store From The Data Keys*

(1) Stop clock if in RUN by depressing START/STOP key
(2) Set test mode switch to EA
(3) Set required address on data keys ,0—15 plus, (X14- X15;4080)(X13 - X15;4070)(X12 - X15;4082)
(4) Depress START/STOP. The address is stored in the BMC
(5) Depress START/STOP
(6) Set test mode switch to W
(7) Set Data on keys
(8) Depress START/STOP. Data will be continuously written into the specified store location.
(9) Depress START/STOP

If a single write operation is required STOP mode switch should be set to IS. Steps 5 and 8 are then omitted.

(f) *For Writing Halfwords In Store Sequentially*

(1) Depress START/STOP key if in RUN
(2) Set STOP mode switch to IS
(3) Set Test mode switch to EA
(4) Set up store address on keys ,0-14 plus,(X14 - X15;4080)(X13 -X15;4070)(X12-X15;4082)
(5) Depress START/STOP
(6) Set up data on keys (0 - 15)
(7) Set Test mode switch on WI
(8) Depress START/STOP once. BMC Store Address Register is incremented after writing data
(9) Set up data as for next halfword
(10) Depress START/STOP once

Repeat 9 and 10 as required

(g) *For Reading Halfwords From Store Sequentially*

(1) Repeat sequences 6.2 f,1 to 5 to define starting address
(2) Set data monitor switches to 07 (Data from store)
(3) Set test mode switch to RI
(4) Depress START/STOP once
(5) Data lamps (0-15) display data read from store
(6) Depress START/STOP once for each successive halfword

(h) *Simple Store Testing*

(1) Writing - Following sequence in 5.2.f steps 1 to 8 but with STOP mode switch in the 0 position. Data from keys will be written throughout the store. (See NOTE 1)

(2) Reading - Following sequence in 6.2.g but with STOP mode switch in the ST position will read all locations in sequence. If a store error is detected the test will be stopped, with store address indicating failing address + 2. Address selection switch = 70. (See NOTE 1)

(j) *Obeying Instructions From Keys*

(1) Halt machine if necessary

(2) Set address selection switch to 41 (IA Register)

(3) Set up in binary the required instructions on the keys

(4) Depress ENTER A

(5) Set STOP mode switch to IS

(6) Set up the halfword instruction operand on the keys. Set test mode switch to OI

(7) Depress START/STOP. Machine will complete the instruction currently loaded

(8) On successive depressions of START/STOP the machine will obey the required instructions

For continuous obey, stop mode switch should be off. Obey 2 takes its operand from store in the normal way. After use a fresh start must be made from RESET

(k) *Entering Microprogram*

(1) HALT machine if necessary

(2) Set address selection switch to 27 (ROM ADDRESS)

(3) Set up required ROM address on data keys (6 to 15)
See NOTE below

(4) Depress ENTER A

(5) Set stop mode switch to MICROSTEP

(6) Depress START/STOP once to execute previous control word

(7) On successive depressions of START/STOP the machine will step in from the specified ROM address

(l) *Stopping Machine At Specified ROM Address*

(1) STOP machine if in RUN

(2) Set up required address on data keys (6 - 15)

(3) Set STOP mode switch to SYNC. STOP (See NOTE 2)

(4) Set Address selection switches to 27

(5) Depress START/STOP

(6) Machine will stop one microstep after ROM address set up on keys

(m) *Stopping Machine At Specified Virtual Store Address*

Repeat 6.2.l steps 1 to 6 but with address selection switches set to 21 and data keys 0 - 14 specifying virtual store address.

NOTE 1: If an attempt to access beyond the top store is made the store error lamp is lit.

NOTE 2: When operating machine with SYNC.STOP the BMC may be stopped in the middle of a transfer. It may be advisable to prevent the BMC running by depressing the BMC inhibit key

(n) *Engineers Sync Facility*

A monitor point on the right hand side of the CPU rack provides a sync point for an oscilloscope. When data on the keys coincides with the contents of a register, selected as for the SYNC STOP facility, a sync pulse is available independent of the STOP mode switch.

(o) *Input/Output*

Autonomous transfers can be initiated independent of the CPU by loading the appropriate Way Control Block and I/O Control block in store and triggering the BMC to simulate a direct output command.

(1) Set CPU INHIBIT and BASIC TEST keys down

(2) Using the data keys load the 2nd, 3rd and 4th halfwords of the Way Control Block (WCB) into store. The 1st halfword contains ENTRY and PROCESS No's and is not used. The 2nd halfword is used for STATUS and should be cleared. The 3rd halfword contains the number of bytes to be transferred except for the two most significant bits which are used as the two most significant bits of END ADDRESS. The 4th halfword contains the remainder of the END ADDRESS.

(3) Using the keys load the I/O Control Block. The 1st halfword is loaded into location 48 and contains the Way No. The 2nd halfword is loaded into location 50 and contains the Command word.

(4) Depress TRIG.BMC ensuring machine is not in RESET

(5) Depress START/STOP

The BMC will output WAY No. and COMMAND to the controller. If ready it will raise its READY line and an autonomous transfer will commence in the normal way. At the end of the transfer STATUS byte will be written from the peripheral into the most significant byte of the 2nd halfword and the BMC will return to its rest state with its interrupt line true.

Examples:

(a) To load 1024 bytes from a P.T. Reader on Way 0 in binary mode and place in store in locations 140 to 1163 inclusive.

Address (dec:/hex:)	Data (hex:)
130 – 00082	0000 - status bytes cleared
132 - 00084	0400 = 1024
134 - 00086	048B = 1163
48 - 00030	0000 - Way 0
50 - 00032	0040 - Input binary mode

Status byte Addr 130 = 40 after transfer

(b) To output to teleprinter on Way 2 in binary mode 28 bytes from address 0

Address (dec:/hex:)	Data (hex:)
146 - 00092	0000
148 - 00094	001C
150 - 00096	001B COUNT = 28 LAST ADAR = 27
48 - 00030	0002 - Way 2
50 - 00032	0080 - Output binary mode

Useful constants for using this facility.

A typical Way No. allocation might be:-

	WAY	WAY AD Dec:	Hex:
PTR	0	128	80
PTP	1	136	88
TTY	2	144	90
LPTR	3	152	98

	Command Dec:	Hex:	Status for successful transfer Dec:	Hex:
IN CHAR	71	47	129	81
IN BIN	64	40	64	40
OUT CHAR	129	81	64	40
OUT BIN	128	80	64	40
BWA	193	C1	64	40

Table 1: DATA MONITORING

Switch: DA	DB	LAMP: LS	MS0	MS1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0				0								L							15
0	1				0								Z							15
0	2				0								Y							15
0	3				0								S							15
1	0				0								W1							15
1	1				0								W2							15
1	2				0								W3							15
1	3				0								X							15
2	0		MS0	BM MS1	0								BM							15
2	1		MS0	BL MS1	0								BL							15
2	2		MS0	AM MS1	0	HARDWARE ERROR							NUCLEUS AM							15
2	3		MS0	AL MS1	0	MARKERS							LOCATION CODE AL							15
2	4				0	HERROR 3			0	NULOC 2						FM	N	Z	OF	CA
3	0	LS	MSO	Q1 MS1	0								Q1							15
3	1	LS	MSO	Q2 MS1	0								Q2							15
3	2	LS	MSO	Q3 MS1	0								Q3							15
3	3	LS	MSO	Q4 MS1	0								Q4							15
4	0	LS		U1	0								U1							15
4	1	LS		U2	0								U2							15
4	2	LS		U3	0								U3							15
4	3	LS		U4	0								U4							15
5	0	LS		MR	0								MR	(M1) MAIN REG HIGHWAY						15
5	1	LS	MSO	QR MS1	0								MANTISSA SIGN QR	Q–REG HIGHWAY						15
5	2		MS0	AU MS1	0								AU£							15
6	0		0	C1-MODE 1	0	M5£						7	0	C1-ADDR 2	See Note 1					
6	1		MS	KREG 0	1	KREG						7	MS	0	EREG					7
6	2	LS		UR	0								UR	U – REG HIGHWAY						15
7	0		0–6	D 7	8	D						15	2	EMIT		7	See note 2			
7	1				0								M3							15
7	2				0								M4							15
7	3				0								M5£							15

SIMTIC

	11 BMC	12	13	14	15
Note 1	SELECT	C.I. RESPONSE £/0	RESPONSE	C.I. ACTIVE £	C.I. INTERLOCK£
Note 2				C.P. BUSY £	INT (INTERRUPT)

Table 2: ADDRESS MONITORING

Switch: AA	AB	LAMP	X12	X13	X14	X15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0		0	BASE NST 0 (MS)										11	0	RANGE NST 0						7
0	1		0	BASE NST 1 (PV)										11	0	RANGE NST 1						7
0	2		0	BASE NST 2 (SST)										11	0	RANGE NST 2						7
0	3		0	BASE NST 3 (SBA)										11	0	RANGE NST 3						7
0	4		0	BASE CST 0										11	0	RANGE CST 0						7
0	5		0	BASE CST 1										11	0	RANGE CST 1						7
0	6		0	BASE CST 2										11	0	RANGE CST 2						7
0	7		0	BASE CST 3										11	0	RANGE CST 3						7
1	0						0	VA NST 0														15
1	1						0	VA NST 1														15
1	2						0	VA NST 2														15
1	3						0	VA NST 3														15
1	4		0	HP CST 0		3	0	VA CST 0														15
1	5		0	HP CST 1		3	0	VA CST 1														15
1	6		0	HP CST 2		3	0	VA CST 2														15
1	7		0	HP CST 3		3	0	VA CST 3														15
2	0		0	BASE HSR				(NST)						11	0	RANGE HSR						7
2	1		0	HP		3	0	VA														15
2	3		WIDTH X12(4082)	X13	X14	X15	0	SA														15
2	5						FORMAT ATOD							3	BROMS							14
2	7													0	RADE	1	7	RAD				0
4	0						0	DINM£						7	0	DINL£						7
4	1						0	IA														15
4	2						1	RA				6	1	RB			6	0	SCALE			3

AA;AB	ROUTE 2	0	3	
	Switch Setting 26 Waveform	Switch Setting 24 Waveform	Switch Setting 43 Waveform	LAMP
			OPS0	0
			OPS1	1
	BRANCHSEL 1	CMA1	OPS2	2
	BRANCHSEL 0	CMA2	OPS3	3
		CMA3	IBCOMPARE	4
		CMA4	IBFORMATA	5
	NEWAD£9	CMA5	IBFORMATL	6
	NEWAD£8	CMA6	IBFORMATRR	7
	NEWAD£7	CMA7	RBA5£	8
	NEWAD£6	CMB1	RB (A3+A4+A5)	9
	NEWAD£5	CMB2	IBFO£	10
	NEWAD£4	CONDTRUE	IBF1£	11
	NEWAD£3	CMB4	IBF2£	12
	NEWAD£2	CMB5	IBF3£	13
	NEWAD£1	CMB6	IBF4£	14
	NEWAD£0	CMB7	IBF5£	15

Table 3: INSTRUCTION DECODE BD. 109 AND ROMAD BD. 101

BD102

ROUTE 0	1	2	3	
Switch Setting 30 Waveform	Switch Setting 31 Waveform	Switch Setting 32 Waveform	Switch Setting 33 Waveform	LAMP
M3 S2	M78 S0	M5 S2	M11E£	7
M3 S1	M69 S1	M5 S1	M11S0	8
M3 S0	M69S0	M5 S0	M10S1	9
M4 S2	SHIFT 1	M5 EQ to 7£	M10S0	10
M4 S1	LOADSLSR	M5 E12to15£	EXPS1	11
M4 S0	SD 1	EKCONTROL	EXPS0	12

ROUTE4	5	6	7	
Switch Setting 34 Waveform	Switch Setting 35 Waveform	Switch Setting 36 Waveform	Switch Setting 37 Waveform	LAMP
FORMAT A	READ W£	RASEL A	MS	7
FORMAT B	READ LSYZ£	RASEL B	LMS	8
MRRDSEL A1	READ A£	URDSELB1	EMITM/0	9
MRRDSEL A2	RAEQW or X	URDSELA	EMITM/1	10
MRDDSEL B1	RAEQLSY or Z	M15E£	EMITM/2	11
MRRDSEL B2	RAEQA or B	CONDPOS	BYTE	12

Table 4: CONTROL A

AA;AB

BD103

0 Switch Setting 30 Waveform	1 Switch Setting 31 Waveform	2 Switch Setting 32 Waveform	3 Switch Setting 33 Waveform	LAMP
BROM 0	AUS 0	FREG1/11	QUOT A	X14
BROM 1	AUS 1	FORMAT E	QUOT B	X15
BROM 2	AUS 2	COUT REG	CONDZA	0
BROM 15	AUS 3		COND ZC	1
BROM 16	AUMODE	EROM 55£	COND ZD	2
BROM 30	AUCIN	FREG£ 1/12	'1'	3
BROM 31	BROM 40	TSREG/1	'1'	4
BROM 32	BROM 41	—	COND FM	5
BROM 33	BROM 42	GREG£ 1/0	SAC	6

4 Switch Setting 34 Waveform	5 Switch Setting 35 Waveform	6 Switch Setting 36 Waveform	7 Switch Setting 37 Waveform	LAMP
LOAZD or ZB	MAP ABS	M2 AS2	SPRI	X14
LOADOFA£	MAP SEL0	M2 BS2	EROM40£	X15
LOADOFB	MAP SEL1	M2 AS1	EROM41£	0
LOADOFC	LOADMAP	M2 BS1	'1'	1
ENABLEZ£	MAPCST	M2 AS0	OPSCALE0£	2
LOADOFG	LOADCR	M2 BS0	OPSCALE1£	3
LOADOFJ	LOADNORMS1	M2 MSS0	OPSCALE2£	4
'1'	LOADNORMS0	M2 MSS2	OPSCALE3£	5
LOADSD	SET IBE	URDSELA	SET RB2	6

Table 5: CONTROL B

BD111

0 Switch Setting 24 Waveform	1 Switch Setting 25 Waveform	2 Switch Setting 26 Waveform	3 Switch Setting 27 Waveform	LAMP
BROM 28	ADDT 1	PROCPERR£	STTOERROR	X14
BROM 29	ADDT 2	BMCPERR£	CITOERROR	X15
CONDREQ	DAT 1	CPSELECTED	ACTIVE£	0
STOREACTIVE	DAT 2	CCSELECTED	INTO (INTERLOCK)	1

Table 6: TIMER

Switch Setting 44 Waveform	Switch Setting 45 Waveform	Switch Setting 46 Waveform	Switch Setting 47 Waveform	LAMP
BROM 17	BROM 21	BROM 25	WRITEHPR	12
BROM 18	BROM 22	BROM 26	WRITEHSR	13
BROM 19	BROM 23	'1'	SET RB2	14
BROM 20	BROM 24	'1'	U WR SELB	15

Table 7: MAIN REGISTER CONTROL

BRANCH

ROMAD BD101

AA ; AB

Switch Setting 50 Waveform	Switch Setting 51 Waveform	Switch Setting 52 Waveform	Switch Setting 53 Waveform	LAMP
BYTE	CORRREM£	IBCOMPARE	PROTFAIL	2
BYTE	IBCOMPARE	RA=AorB	FLAG	3
INTO	RB=AorB	DYNSTOP	'1'	4
SELorRESP£	KREG0/1	KREG3£	KREG6/1	5
KREG MS/1	KREG0/1	IBF0£	CONDN	6
KREG6/1	KREG4to7=0	'1'	SPR	7
KREG0£	KREG2/1	KREG3to7EQ0	KREG4to7=0	8
CORRQUOT	IBCOMPARE	IBFORMATA	'1'	9
RA=W+X	EXTENDED	RA=S	IBFORMATA	10
CONDTRUE	CONDTRUE	CONDTRUE	CONDTRUE	11
RBA5£	EXTENDED	KREG0/1	KREG1/1	12
KREG0/1	KREG1/1	IBF2£	CONDZ	13
KREG7/1	KREG0/1	SOP£1	'1'	14
KREG7/1	KREGMS/1	KREG2/1	KREG3-7=0	15

Switch Setting 54 Waveform	Switch Setting 55 Waveform	Switch Setting 56 Waveform	Switch Setting 57 Waveform	LAMP
RA=L+S+Y+Z	CONDZ	FLAG	INTO £	2
FLAG	RB=A+B	KREG6/1	'1'	3
CONDN	'1'	'1'	OV	4
IBF 5	IBF 5£	CONDN	FLAG	5
CONDNORM	KREG2/1	KREG0/1	K5to7EQ100	6
KREG1/1	K5to7EQ000	START	KREG6/1	7
CONDZ	SAPR/2	INT £	PCINT£	8
RA=W+X	SACNESOP	IBF 3	ODDPARITY	9
RA=W+X	RA=S	K5to7EQ000	'1'	10
CONDTRUE	CONDTRUE	CONDTRUE	CONDTRUE	11
KREG3/1	CONDNORM	CONDZ	CONDN	12
EXTENDED	KREG3/1	EXTENDED	KREGMS1	13
KREG2/1	K5to7EQ010	SENSE1	K5to7EQ000	14
KREG5/1	SACNESOP	SOP/1	INT	15

Table 8: CONDITIONS

DA; DB

Switch Setting 06 Waveform	Switch Setting 16 Waveform		Switch Setting 26 Waveform	Switch Setting 36 Waveform	Switch Setting 07 Waveform		LAMP
IOSA 0	PER 0		IOC 0	PER 0	SD 0		0
IOSA 1	PER 1		IOC 1	PER 1	SD 1		1
IOSA 2	PER 2		IOC 2	PER 2	SD 2		2
IOSA 3	PER 3		IOC 3	PER 3	SD 3		3
IOSA 4	PER 4		IOC 4	WA 4	SD 4		4
IOSA 5	PER 5		IOC 5	WA 5	SD 5		5
IOSA 6	PER 6		IOC 6	WA 6	SD 6		6
IOSA 7	PER 7	INFO IN	IOC 7	WA 7	SD 7	DIN	7
IOSA 8	PER 8		IOC 8	WA 8	SD 8		8
IOSA 9	PER 9		IOC 9	WA 9	SD 9		9
IOSA 10	PER 10		IOC 10	WA 10	SD 10		10
IOSA 11	PER 11		IOC 11	WA 11	SD 11		11
IOSA 12	PER 12		IOC 12	WA 12	SD 12		12
IOSA 13	PER 13		IOC 13		SD 13		13
IOSA 14	PER 14		IOC 14		SD 14		14
IOSA 15	PER 15		IOC 15		SD 15		15

Switch Setting 46 Waveform	Switch Setting 56 Waveform		Switch Setting 66 Waveform	Switch Setting 76 Waveform	LAMP
SD 0	PER 0		IOSA 0	READY 0	0
SD 1	PER 1		IOSA 1	READY 1	1
SD 2	PER 2		IOSA 2	READY 2	2
SD 3	PER 3		IOSA 3	READY 3	3
				READY 4	4
				READY 5	5
				READY 6	6
				READY 7	7
				READY 8	8
				READY 9	9
				READY 10	10
				READY 11	11
OUT ENABLE			SIG 12	READY 12	12
RE 13	ERR 13	See BMC User Manual.	SIG 13	READY 13	13
RE 14	ERR 14		SIG 14	READY 14	14
RE 15	ERR 15		SIG 15	READY 15	15

Table 9: DATA MONITOR HIGHWAY

AA:AB	Switch Setting 70 Waveform	Switch Setting 71 Waveform	Switch Setting 72 Waveform	LAMP
	SXADD 14			X14
	SXADD 15			X15
	SADD 0		SM I0 } STATICISED	0
	SADD 1		SM I1 } MODE IN	1
	SADD 2		IM I0	2
	SADD 3		IM I1	3
	SADD 4		PROCEED	4
	SADD 5		OUTTIME	5
	SADD 6		ENGAGE	6
IOSA	SADD 7		INTIME	7
IOSA	SADD 8			8
IOSA	SADD 9			9
IOSA	SADD 10	ROMAD 0	MODE OUT 0£	10
IOSA	SADDD 11	ROMAD 1	MODE OUT 1£	11
IOSA	SADD 12	ROMAD 2	LW£	12
IOSA	SADD 13	ROMAD 3	BURST	13
IOSA	SADD 14	ROMAD 4		14
IOSA	SADD 15	ROMAD 5		15

Table 10: ADDRESS HIGHWAY (BMC)

NOTE:

For Store Address (SADD) SYNC. STOP use keys X14, X15, 0-15

For ROM Address (ROMAD) SYNC, STOP set. keys X14, X15, 0-9 to '0' and use keys 10-15

} 4080

For Store Address (SADD) SYNC, STOP use Keys X12 to X15, 0-15.

For ROM Address (ROMAD) SYNC, STOP set Keys X12 to X15, 0-15,

} 4070 and 4082