PDP 5

DIGITAL EQUIPMENT CORPORATION

PROGRAMMED DATA PROCESSOR-5

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PDP-5 FOR

SYSTEMS CONTROL
DATA CONTROL
DATA COLLECTION
DATA REDUCTION
FORMAT CONVERSION
DIGITAL TRAINING

Digital's Programmed Data Processor-5 answers the need for a low cost, high reliability digital computer to be used either as an independent information handling facility or as the control element in larger systems.

The PDP-5 is a single address, fixed word, stored program computer operating on 12-bit, 2's complement binary numbers. It has a 6 microsecond memory cycle time and fully parallel processing, which provide a computation rate of 55,555 additions per second.

The interface is extremely flexible, accommodating a wide range of external devices, and there is ample provision for future expansion.

The use of solid state components and provision for marginal checking help to assure machine reliability, even under extreme operating conditions.

The basic PDP-5 system includes the Central Processor, 1024 or 4096-word random access Magnetic Core Memory, Printer-Keyboard and Perforated Tape Reader-Punch, and Input-Output Control. Standard features include a complete order code structure, indirect addressing, data interrupt, and program interrupt.

STANDARD PDP-5

The standard Programmed Data Processor-5 is contained in a single bay. Additional bays are available to accommodate options ordered or planned. The major components of the basic computer are:

INTERNAL PROCESSOR

carries out arithmetic operations, provides memory access and controls information entering or leaving the machine. It consists of the six registers and two information handling elements.

MEMORY ADDRESS REGISTER (MA) — used to address a word in memory; provides addressing for 1024 or 4096 words of memory.

MEMORY BUFFER REGISTER (MB) — holds information which is being written into or read out of the core memory.

INSTRUCTION REGISTER (IR) — contains the instruction currently being performed by the machine.

ACCUMULATOR (AC) — performs the arithmetic operations, together with the Memory Buffer Register.

CARRY LINK (L) — used to extend the capabilities of the Accumulator; greatly simplifies multiple precision arithmetic.

SWITCH REGISTER — contains the word to be deposited in the Memory Address Register or Core Memory or to be read into the Accumulator under program control.

INPUT MIXER — allows information to be fed into the Accumulator.

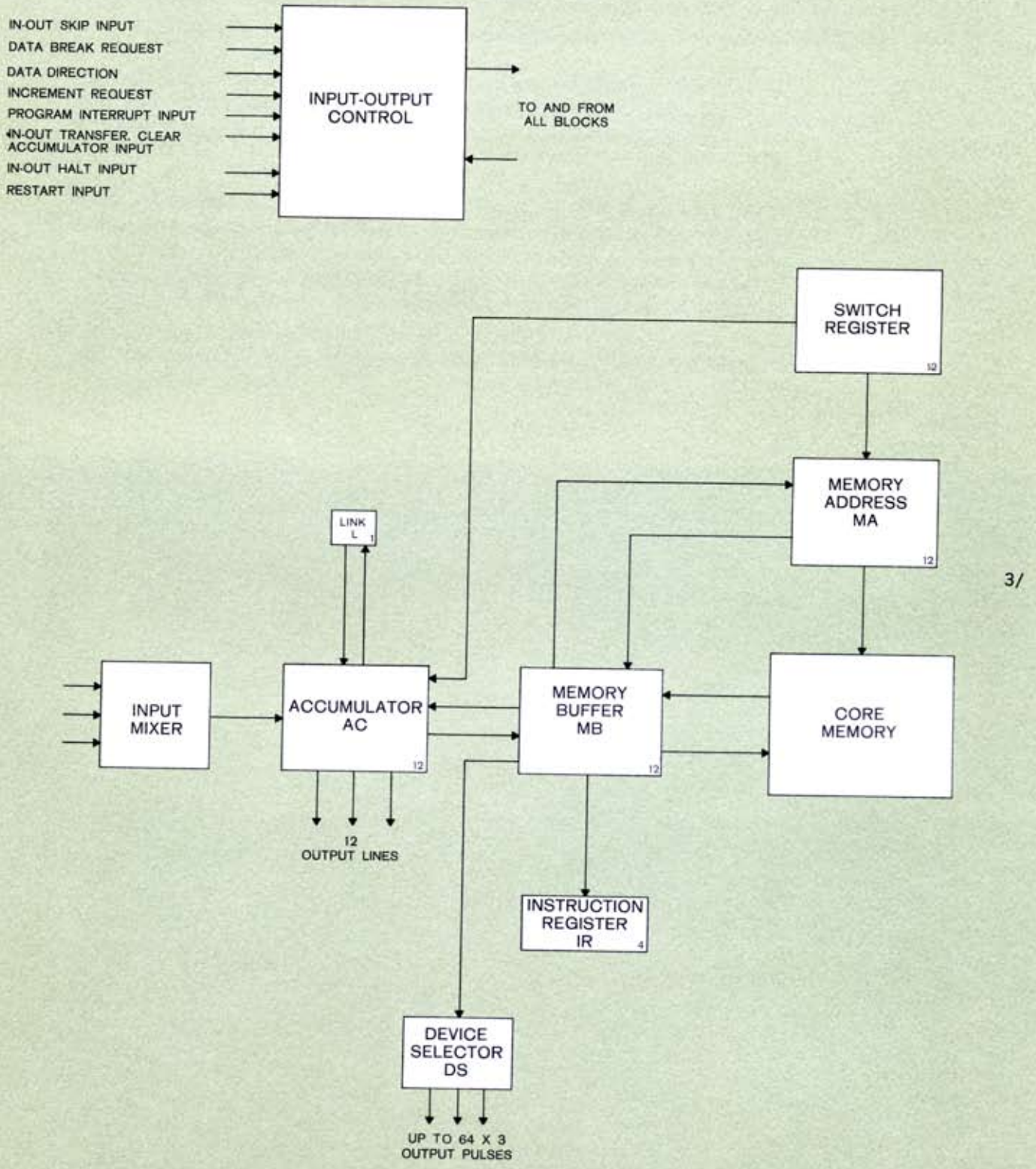
DEVICE SELECTOR (DS) — produces pulses which transmit information through the Information Distributor or read in information through the Input Mixer.

OPERATOR CONSOLE

contains the indicators, keys and switches to operate the machine and to observe and modify the status of the Internal Processor. The functions of the keys and switches are described on Pages 4 and 5.

MEMORY

provides storage for instructions to be performed by the Internal Processor and holds information being collected or distributed. This is a random access, magnetic core memory available with either 1024 or 4096 words.



PDP-5 BLOCK DIAGRAM

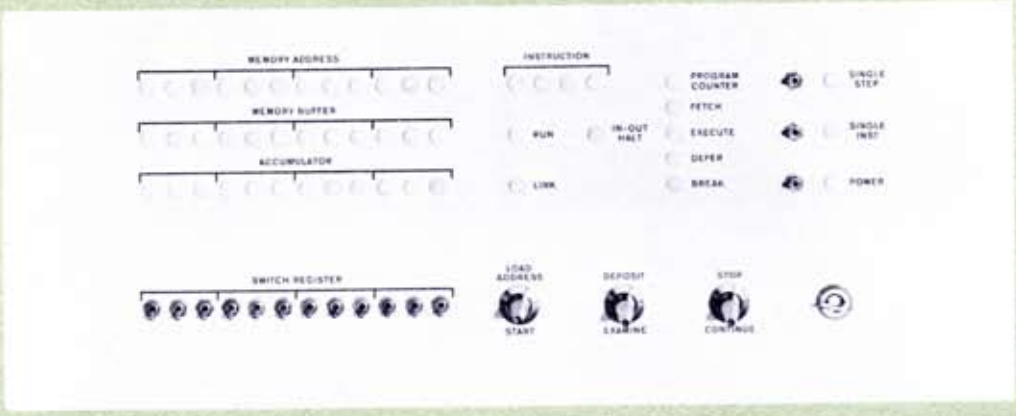
INPUT-OUTPUT CONTROL

a means of transmitting data to or receiving data from external devices. It has several different classes of inputs.

DATA BREAK — permits the transmission of data directly to core memory. It includes three types of requests — Data Break Request, Data Direction, and Increment Request. An Increment Request transfers the next block of data to the next address without respecifying.

PROGRAMMED IN-OUT — makes it possible to specify iot instructions which affect the state of selected devices. The iot instruction is micro-programmed to allow one basic instruction to handle many devices. The command pulses occur at various times to allow flags to be sampled (and an instruction skipped), buffers to be cleared, and data to be transmitted to or from the Accumulator.

IN-OUT SKIP INPUT (IOS) — allows computer programs to skip according to selected extra machine states.



All keys, switches and indicators are located on a convenient control panel just above the console shelf on the front of the PDP-5.

CONSOLE KEYS

START	Starts computer. The first instruction is taken from the memory at the address presently in the memory address register.
STOP	Causes the computer to stop at the completion of the memory cycle in progress at the time of key operation.
CONTINUE	Causes the computer to resume operation at the point where it left off.

IN-OUT HALT — permits the computer to be halted during the time external devices are operating and then restarted by a pulse from the device.

IN-OUT TRANSFER, CLEAR ACCUMULATOR INPUT — enables the buffers to be cleared.

PROGRAM INTERRUPT INPUT — allows external devices to interrupt the computer program under certain predetermined conditions.

STANDARD INPUT-OUTPUT

a Printer Keyboard and Tape Reader-Punch unit permits the operator to receive data from or send it to the Internal Processor. It is standard Teletype equipment with a speed of 10 characters a second.

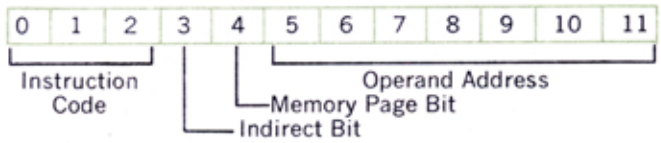
EXAMINE	Sets the contents of the memory cell selected by the memory address register into the accumulator and the memory buffer. The memory address register will then be incremented by one.
DEPOSIT	Sets the word selected by the switch register into the memory at the location specified by the memory address register. The results will remain in the memory buffer. The memory address register will then be incremented by one.
LOAD ADDRESS	Deposits the contents of the switch register in the memory address register.

CONSOLE TOGGLE SWITCHES

SWITCH REGISTER	Contains a word to be manually deposited into memory or into the memory address register by means of the load address or deposit keys. The contents of the switch register may also be brought into the accumulator under program control.
SINGLE STEP	Causes the computer to halt at the completion of each memory cycle. Repeated operation of the CONTINUE key will step the program one cycle at a time so that the state of the machine can be examined at each step.
SINGLE INSTRUCTION	Causes the computer to stop at the completion of each instruction.
POWER	Turns on power.
LOCK SWITCH	Disables all keys on the console and turns on the power.

PDP-5 INSTRUCTIONS

The PDP-5 instruction format includes three bits for the instruction code, one bit for indirect addressing, one bit for memory page addressing, and seven bits for the address of the operand.



When the indirect bit is a ONE, indirect addressing (or deferring) is specified. A defer memory cycle is required during which time the contents of the memory cell addressed is selected and the entire contents of this cell are used as the effective address of the original instruction. In addition, if the cell indirectly addressed is 10_8-17_8, a ONE is added to the contents of that cell before they are used as the effective address.

Instruction execution times are multiples of the 6-microsecond cycle time. Jump, in-out transfer and operate are performed in 12 microseconds; and, add, index and deposit take 18; jump to subroutine requires 24.

In the memory addressing scheme for PDP-5, memory is considered to be divided into blocks of 128 words. Each block is called a "page," and pages are numbered starting with 0. A directly addressed memory reference instruction may refer to either page 0 or the page on which the instruction is located. If bit 4 is a ONE, the reference is to the page we are presently on. Thus, any instruction may directly address 256 words of memory. All other portions of memory are referred to by indirect addressing. An indirect address refers to a full 12-bit word which may address any cell in 4,096 words of memory.

MEMORY REFERENCE INSTRUCTIONS

Addressable or memory reference instructions are instructions which contain a memory address. The address portion of the instruction word specifies the location of an operand in the memory.

MNEMONIC CODE	OCTAL CODE	OPERATION	TIME (μSEC)
and Y	0	Logical AND. The logical AND function is performed on a bit by bit basis between the contents of the accumulator and the contents of Y. The result is left in the accumulator and the original contents of the accumulator are lost.	18
tad Y	1	2's complement add. The contents of Y are added to the contents of the accumulator in 2's complement arithmetic. If there is a carry out of bit ZERO of the accumulator the link will be complemented. This feature is useful in multiple precision arithmetic.	18
isz Y	2	Index and skip if ZERO. The contents of Y are replaced by the contents of Y plus ONE. The contents of the accumulator are unaffected by this instruction. If the resulting sum is ZERO, the instruction following the isz is skipped.	18
dca Y	3	Deposit and clear accumulator. The contents of the accumulator are deposited in memory register Y. The accumulator is then cleared.	18
jms Y	4	Jump to subroutine. The contents of the program counter contained in register ZERO are deposited in register Y. The next instruction will be taken from Y + 1.	24
jmp Y	5	Jump. The contents of the program counter contained in memory register ZERO are reset to address Y. The next instruction that will be executed will be taken from memory register Y. The original contents of the program counter are lost.	12

AUGMENTED INSTRUCTIONS

Augmented instructions provide micro-programming capability by using the address portion of the instruction to select logical operations. These instructions do not address a memory register.

MNEMONIC CODE	OCTAL CODE	OPERATION	TIME (μSEC)
iot	6	In-out transfer. This instruction is used to select an input or output device. The instruction forms a micro-program and has the format indicated in "In-Out Transfer Instruction Group."	12
opr 1	70		12
opr 2	74	Operate. The operate instruction is a micro-programming instruction; that is, various actions are specified by individual bits of the address portion of the instruction. Within certain limitations, several actions can be called for in the same operate instruction. The operate is also the conditional skip instruction. When a particular condition is present, the following instruction will be skipped. Since the operate instruction is not deferrable, the indirect bit 3 is used to specify two classes of operate instructions. The operations are specified by bits as indicated in "Operate Instruction Group."	12

OPERATE INSTRUCTION GROUP

These instructions use bits 5 through 11 to specify variations of the basic instructions.

MNEMONIC CODE		OPERATION	OCTAL CODE OF ADDRESS PART	SEQUENCE OF OCCURRENCE
opr 1	nop	No Operation	0	
	cla	Clear Accumulator	200	1
	cll	Clear Carry Link	100	1
	cma	Complement Accumulator	40	2
	cml	Complement Carry Link	20	2
	rar	Rotate Accumulator and Link right one position	10	2
	ral	Rotate Accumulator and Link left one position	4	2
	rtr	Rotate Accumulator and Link right two positions	12	2 and 3
	rtl	Rotate Accumulator and Link left two positions	6	2 and 3
	iac	Index accumulator	1	3
opr 2	cla	Clear Accumulator	200	1
	skp	Skip Unconditionally	10	2
	sma	Skip on − Accumulator	100	1
	sza	Skip on zero Accumulator	40	1
	spa	Skip on + Accumulator	110	1 and 2
	sna	Skip on non-zero Accumulator	50	1 and 2
	snl	Skip on Link equals one	20	1
	szl	Skip on Link equals zero	30	1 and 2
	osr	Or with switch register	4	2
	hlt	Halt	2	1

IN-OUT TRANSFER INSTRUCTION GROUP

The instructions in this group are similar to the Operate Group instructions except they pertain to the transfer of information between the Central Processor and various input-output devices. Bits 3 through 11 select and control input-output devices.

FUNCTION	COMMAND BITS
Specifies the in-out transfer instruction (Operation Code 6)	0-2
Selects the device	3-8
Transfers an IOT pulse at event time 3 if a "one"	9
Transfers an IOT pulse at event time 2 if a "one"	10
Transfers an IOT pulse at event time 1 if a "one"	11

OPTIONAL INPUT-OUTPUT EQUIPMENT

HIGH-SPEED PERFORATED TAPE PUNCH AND CONTROL TYPE 75

Punches 8-hole tape at 63.3 characters a second.

HIGH-SPEED PAPER TAPE READER TYPE 750

Reads perforated paper tape photo-electrically at 300 characters a second.

MAGNETIC TAPE TRANSPORT TYPE 50

Reads and writes IBM-compatible magnetic tape at a transfer rate of 15,000 cps.

AUTOMATIC MAGNETIC TAPE CONTROL TYPE 57A

Automatically controls up to eight Type 50 Magnetic Tape Transports. Provides information transfer through the computer's data interrupt facility. Controls tape reading or writing at a 15,000 cps transfer rate, 200 bits per inch. The tape format is compatible with that of IBM equipment.

OSCILLOSCOPE DISPLAY TYPE 34

Plots data point by point on a Tektronix Oscilloscope Model RM 503 using 10 bits for each axis.

PRECISION CRT DISPLAY TYPE 30D

Plots data point by point on a 16-inch CRT. Ten-bit X and Y coordinates are separately variable.

LIGHT PEN TYPE 32

Detects information displayed on a Type 30D Display and sends identifying signal to the computer.

DUAL MICRO TAPE SYSTEM

Provides a fixed-address magnetic tape facility for high-speed loading, reading, and program updating. Consists of a Type 555 Transport Unit and a Type 550A Control Unit.

INCREMENTAL PLOTTER AND CONTROL TYPE 350

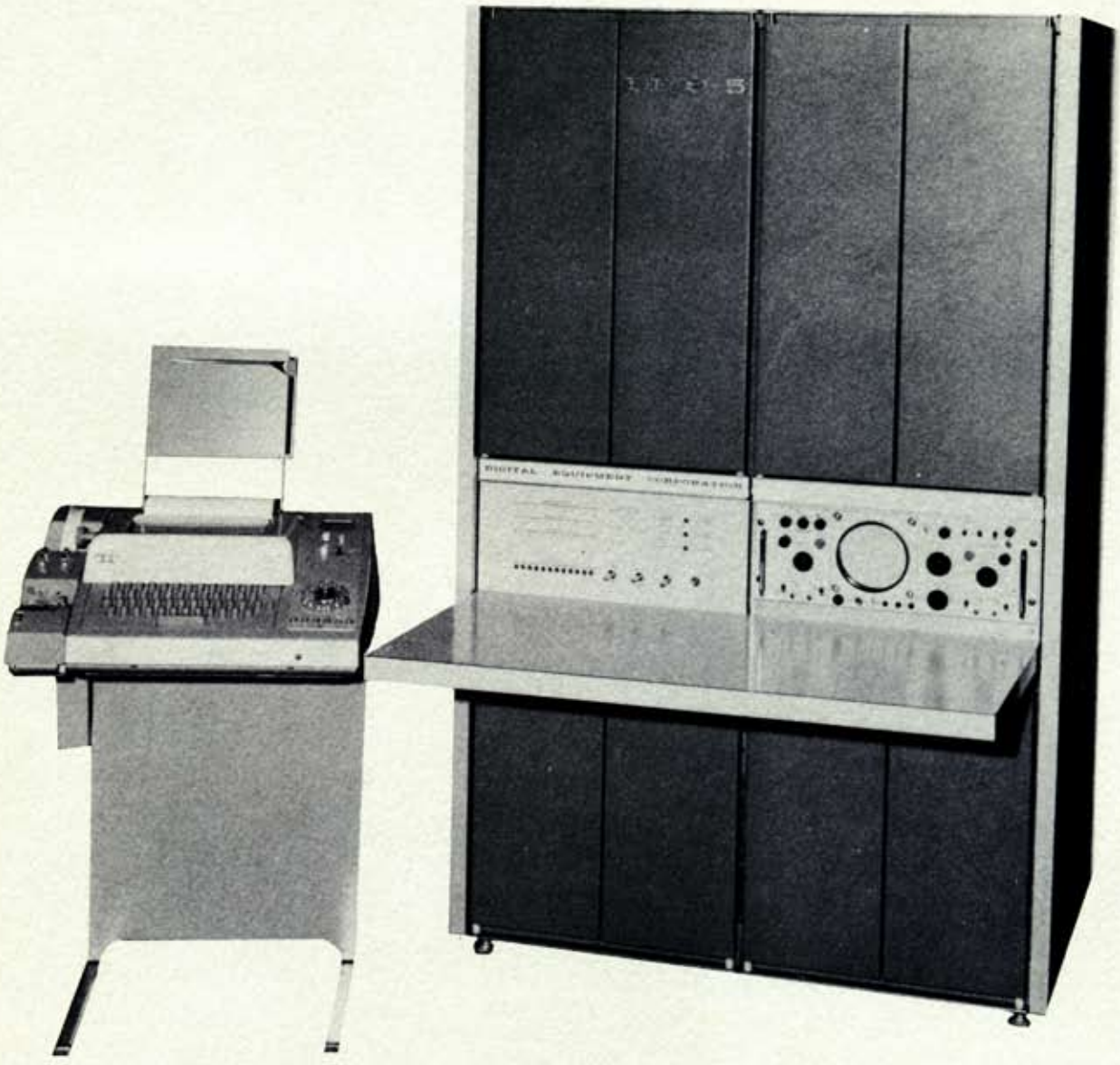
Plots points on chart paper 12 or 31 inches wide.

ANALOG-TO-DIGITAL CONVERTER TYPE 137

Wired into the computer, but modules to activate it are optional extras. Uses the successive approximation technique. Offers accuracy of up to 11 bits, depending on speed required.

ADDITIONAL EQUIPMENT BAY

Accommodates optional equipment requiring more space.



Programmed Data Processor-5 with extra bay in Pulse Height Analyzer configuration

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3553 PRINTED IN U.S.A. 30M 9/63