[[NB03-001]]

61 Belsize Pk

6-7-50.

This morning was spent checking up on the expected consumption of power supplies. The demand upon the 250v [[instability]] has now reached the neighbourhood of 27 amps allowing for the double storage capacity. Other supplies should be sufficient provided that there is no change of policy.

[[NB03-002]]

7.7.50

After so much time spent on negative multiplication it seems strange to have found at this stage yet another cause for the introduction of additional “1”s. However another cause has been found. It was noticed that even after the AD1 [[I^5I^5]] had been restored to normality that errors in the shape of spurious “1”s in the less sig. half of the ~~ord~~ acc. were still appearing at times, but having got the correct answer in the acc once all repetition of the multiplication

gave the correct answer.
Even when a wrong answer was arrived at the first time so long as something present in the acc to be added to, subsequent answers added in were correct. This suggested zero restoration trouble and this fault was quickly located to the second half adder where the input to the clocking gate was bouncing horribly each time a long string of 1s was added to nothing. At the same time as this fault was being investigated it was noticed that the Acc I was showing signs of

[[NB03-003]]
a broken crystal and as the unclocked pulses at this stage were getting rapidly worse the investigation on the zero restoring fault were curtailed by putting in a new half adder to prove the point. The new half Adder behaved quite well and at last -6 x 7 (-6 in the m[[ultipl]]icand) was reliably performed at last!
Within two hours of first noticing the crystal trouble the Acc I was unusable.
On dismantling the tank it was found that the two crystal were OK but that an alkohol leak had developed behind

one of them. This was a tube in which the ridge on the steel washers had been reduced by about 5 thou by rubbing down.

[[NB03-004]]
Initial input

[[DIAGRAM]]

Action Letter Convert address
Arrange to transfer next No to next position build op order
Transfer to Store

Modification of Orders
1 Note the start of each stage
2 Recognise relative addresses
3 Modify them.

K = start of new stage
F.O.K. ← first order of stage

[[DIAGRAM]]
Action Convert
Note N o of first order last digit?
Arrange build
transfer

[[NB03-005]]

[[DIAGRAM]]
if - numeral
digit -10
-1
---
l Brackets 1 x 1/8 as specimen c/s holes
12 ¾" x 8 screws
12 1½ x 8 screws
12 2BA x ¾" screws + nuts
12 " Washers
Tarpaulin
Rope
8 cleats

[[DIAGRAM]]

Note Ref No Add in ref no

[[NB03-006]]

11-7-50

Yesterday two short tanks which had been showing signs of trouble Acc I & TCT were dismantled & refilled. In both cases the trouble was due to leakage behind the crystal and on reassembly rubber washers were given a smear of vaseline.
With these tanks in operation, today tests were made on all the usual sequences. The one which failed curiously enough was negative multiplication with a negative multiplier for some as yet unknown reason a few 1^s get left out in the

middle of the Acc.

12-7-50

Pursuing the investigation of the fault mentioned above it was noted that even a simple multiplication of 1 x -6 was resulting in the same effect.
The complementer was cleared of blame by multiplying (+1) x (+6) and connecting the contents of the acc to the complementer which then gave repeatedly the correct

answer.
This again suggested that possibly some zero restoration fault in the accumulator loop was the cause. As a step towards investigating this V3 of the two half adders was

[[NB03-007]]
removed, thus preventing any addition effects (in effect converting the Accumulator loop into a 2 m/C store) and repeating the multiplication. Under these circumstances there was no tendency at all to drop out 1's

13-7-50

A little more time spent on the multiplication with a negative multiplier.
The following points have been noticed
(a) If -7 in m[[ultipl]]ier is used to multiply a single 1 of any position in the m[[ultipl]]icand, the correct answer is obtained.
(b) If -7 m[[ultipl]]ier is multiplied by two 1's then the addition goes wrong either a small gap of 1 or 2 pulse widths being left in the middle or else no pulses at all being registered in the more significant half of the

[[NB03-008]]
accumulator.
This fault occurs irrespective of the size of the numbers. Eg. with D23 D24 & D25 as the operative digits ~~subtracted~~ complemented & transferred to the m[[ultipl]]ier & multiplied against itself in the m[[ultipl]]icand gave an answer of
11110011111111011111111 (approx)
~~This suggests that the last (complemented) partial product is going astray and being added in either to early or too late.~~
If this incorrect result is not due to incorrect functioning of the adding circuit then it means that an additional bunch of '1's is being

```
          0000111
          1111001
          0000111
        0000000
      0000000
    0000111
1111111111111001
1111111111111001111
```

added into the more significant half of the accumulator.
But if this is the same fault that was occurring earlier then sometimes a single 1 is likely to be added to produce
0000000 1111111 001111
What simple fault is likely to produce both these errors?

[[NB03-009]]
Possibility that the complement is not all that could be desired in amplitude.

Inspection of the incorrect results from multiplication using negative m[ultipl]ier: -

M[[ultipl]]iers	M[[ultipl]]icands
111111111111001	000000000000111

Correct answer
---111111111111111111001111

Answers obtained

	ss
a	111111111111000111111111001111
b	111111111110010111111111001111
c	111111111111010111111111001111
d	000000000000010111111111001111

This suggests that an incorrect complement is being added in. The correct complement is

1111111111111001

To produce these incorrect answers a number corresponding to

a	1111111111101011
b	1111111111011111
c	1111111111101111
d	1111111111111111

would need to be added in for each different answer.

To confirm correct functioning of the complementer the positive part of the product was prevented from flowing to the accumulator by removing the 37' input to the Acc IO. The total arriving via the complementer was the correct complement as above.

To complete this test the complement~~er~~ was suppressed

[[NB03-010]]
by disconnecting from HAI z terminal & here, apparently is the trouble. & the 37' connection remade The totals repeatedly obtained were

0000011111111001111
Sbe 0000 11011111111001111

Not only this, but when the multiplication was allowed to repeat there was no building up of the more significant end of the number except for spasmodic “1”s here & there suggesting that there was some sort of suppression pulse being applied to prevent carries past a certain point. It now seems that instead of the negative part of the number going wrong it is the

positive.

This suppression effect seems to happen always after the first batch of “1”s in the positive part of the product. This coincides with the setting up of the W4 waveform.

- - - -

W4 waveform suppressed by removing C 14 from 32^4 everything O.K.

W4 + [[&]] - suppressed in turn If both are suppressed (by disconnecting from leads going away from 32^{8+9}) the positive part of the multiplication is OK but if either W4 + or - is connected up errors occur.

[[NB03-011]]
If however W_4- only is disconnected and also the complement connection to half adder is ~~also~~ disconnected then once again the positive part of the answer is OK With W_4- only connected and comp output disconnected then the answer is still wrong.

Trouble can be due to
(a) Suppression of the end of the positive part of the number
(b) The addition of a negative number which cancelled that part of the +ve answer which is missing.

17-7-50.
Trouble on complementer apparently due to zero restoration again. This has now been modified to come in line with Half Adder Mod.

[[NB03-012]]
Notes on Possible Reciprocation Sequence
(a) Resulting in dividend in the multiplicand & remainder in the accumulator.
i) x into multiplier, D_1 into Acc (more sig) first digit of m[ultipl]ier starts ~~some~~ TCT pulse W3 suppressed, ~~W2 applied to Left shift gates of acc.~~
ii) m[ultipl]ier subtracted or added to accumulator at every second minorcycle according to whether acc is - or +. For every + a D_1 sent to m[[ultipl]]icand.

Additional equipment required to effect following.
1. 0 D_1 into accumulator
2. Stimulating pulse (could be as for ' multiplication in which case paths of division must be switched)
3. 1^5 1^5 to be triggered for left shift.
4. Discrimination between + & - in acc.
5. "1" ^{5} for quotient.
6. Access to quotient.

Possibilities
1. S pulse
2. as for mult
3. New DC FF with new mixer in ACC SU II ~~before~~ after S1
4. P_R gets new FF

[[NB03-013]]

19-7-50.
Trouble on Complementer is as follows:-
Having set up complementer for maximum amplitude output & minimum breakthro using a repetitive number recurring every two minorcycles, it is found that using it on single shots errors are produced as seen by adding into accumulator or a store. If P_2 is now adjusted to give consistently correct results on single shots basis and then the input is made repetitive, the output is seen to have considerably more breakthro (up to [[4]] volts) This is not satisfactory as it

suggests that the Complr is being used on the fringe of its controls.

Negative multiplication
Returning to multiplication using a negative multiplier $W_4\pm$ was connected via loose leads so as to avoid any capacitive coupling to other leads on the rack. Results were precisely the same as before

[[NB03-014]]
It was found that the same trouble in neg mult was experienced for all numbers and to avoid difficulty in counting the “1”s decided to use D22 to 24 x [[illegible by?]] D33 & D35 In this way W_4 could be inspected on triggered scope by using W_3 on a synch.

Examination of output of Collater & Mixer showed that there was excessive breakth from the gate that should be closed by W4-. This was eventually found to be due to an insufficient large W_4 waveform which did not quite reach the +10 volt

from the 35v to which it had been restored. This was overcome by restoring to 30 volts.
After this mod multiplication of all kinds were successfully performed 7 x -7 = -49
-7 x 7 = -49
-7 x -7 = +49
I think that this fault may well be due to insufficient amplitude of the FF output from the S.P.G. assist which W4 is gated in CCU VIII ie the mod my not be necessary when using a large coder waveform as will be obtained from the Static Registers.

[[NB03-015]]

20-7-50

Multiplication with -ve mier is still going wrong for long negative numbers but it has been assumed that this is due to insufficient amplitude of waveform from S.P.G and should be OK with standard Coder Waveform.

X & Y Order.
X worked first time but Y did not. Found to be due to insufficient amplitude of $1D_0$ (Odd D_0 gated twice + mixer + CF) Temporarily corrected by eliminating CF but this to be replaced and an amplifier inserted

Acc Transfer & Clear. T.
Using an even D_1 in place of R_2 pulse (no coord) this worked first time

---

21-7-50.

Panel 39 CCU IX brought in to operation to clear multiplicand and multiplier tanks
A delay was necessary in the $S_1 + S_2$ line to permit its being gated by a Coder Waveform.
Both these clearing waveforms worked first time.

[[NB03-016]]

[[diagrams of trailer hitches]]

8" x 24"

Mud guards.
16 swg Aluminium

[[diagram of trailer]]

(a) width of woodwork 2' 10"
(b) length 4'
(c) height 1'
(d) Wheel Diameter 2' 3"
(e) length of towing tackle 1' 11"
(f) outside of wood to outside of wheel 5"
(g) Width of one plank 5½"

Overall length 6'
Width 3' 8

[[NB03-017]]

24-7-50

Acc1 showing signs of leak again. Dismantling confirmed this. Reassembled with new steel washers taken from an unused tank. Should be ready for work tomorrow. This lays us open to a possibility of broken crystals but until a new washer has been designed we are obliged to take this risk in order to keep the computer going.

Consideration preliminary to testing Coordinator + Coinciden units.
1.) Transfer Units & Tanks tested & connected up.
2.) Static Registers & Action decoders including primary action decoders working.
3.) ~~Operated~~ Coder working
(4) Operate Computer direct from order simulating order on number simulator
(5) Set up Counter tank & Sequence Control tank with half Adders.
(6) Set up Order tank.

[[swirl doodle]]

[[NB03-018]]
7) Set up one panel 1 connected to a long tank.
8) Tank No Static registers & tank No Decoders required.
(9) Check to select correct tanks
~~10)~~
All above tests prior to Use of Coord & Coince units.

Alternatively work could proceed with Coord & Coince while wiring check & prelim test on Static Registers etc are proceeding.

Priority on Work
1. Raster Scope
2. Wiring of Coord.
3. Static Registers
4. Transfer Units
5.

25-7-50

Testing period of Computer now coming to an end. We have decided not to be disturbed by any minor apparent fault ~~that is likely~~ on sequences already tested but used again in testing other sequences as these may well be due to shortcomings of the SPG or other testing condition such as long limp coder leads & insecure croc clips

[[NB03-019]]
Sequences that have been tested now are X Y E & G. & the only minor snag encountered is that the P_g pulse requires amplification and this can be provided in the CCU X
One bother than constantly arises is the low amplitude of odd & even pulses. In any future major mod it would be a definite advantage to have these amplified up to standard pulse amplitude.

Preparation

1) ~~Fix Mudguards~~	1) Nails & Screws
2) ~~Coat Paint.~~	2) Hammer
3) ~~Cleats~~ & T [[symbol]]	3) Padsaw.
4) Rear light.	4) Eclipse Saw.
5) [[Primers]]	5) Small stool
6) ~~Boxes for larder~~ & ~~stove.~~	6) Bats & Balls
7) ~~Paint from work or Touring fixtures~~	7) Kite & cord
8) Examine Tent & get any extras.8)	
9)	

[[NB03-020]]

26-7-50

Computor testing virtually comple[[ted]] attention was given today to the pulse shapes. Pulse shapes of clock pulses in particular had been very bad & this was found to be due to a variety of causes.
(1) No proper termination to the clock I in the Clock & Digit Distrib Unit. These have now been inserted.
2.) Bad bonding between rows of racks. It appears now that it will be desirable to bond up the racks at the top row to row as well as rack to rack.
3.) The impedance of the line varies from point to point due to the

fact that in some cases it passes quite close to the rack framework while at other points it is isolated in air. In some measure this was improved by substituting a thick wire between the CP generat[[or]] rack and the row of computor racks thus reducing the impedance of a line which is mainly in free space

[[NB03-021]]
Suggested Future Programme
Tests on Computer having been satisfactorily completed, the following programme is suggested :-

A. COORD. CONTROL
1) Complete pulse wiring of Coord Racks

2) Bench tests on Coord Control Units

B. COINCIDENCE UNITS
1) Pulse wiring
2) Bench tests
3) Counter Tank + ½ Adder

C. COORD. + COMPUTER
1) Pulse Wiring

2) Mods to Computer
3) Bench tests on S.R.'s, Recoders, P.F.D, & Coder
4) Computer to work with proper Coder waveforms with coded order set up on Nº simulator

D. O.T. & S.C.T + ½ Add.

E. TRANSFER TANK & UNITS + L/S. S.R.

By this time a Storage Battery should be available for use with Coince Unit

[[NB03-022]]
Priority of Jobs

1. Pulse wiring
2. Computer mods.
3. Complete bench test on Coord and Coince Units
4. Bench tests on S.R.'s, Recs & Coder.
5. Raster Scope.
6. Coord rack tests
7. Coince Unit rack test
8. [[Computer]] sequences using SR's decoders etc.
~~9.~~ working from Nº simulator in place of O.T.

Fri Aug 11 th

All mods to computer rack wiring & units complete. 4 Coordinator control units & 2 Coince Units have been tested by Shaw & Gibbs has just finished Coord. wiring. We are now ready to begin Coord tests

[[NB03-023]]

Monday Aug 14 1950

Work commenced on Rack tests of the Coordinator
Panel 9 and part of Panel 10 tested by feeding S_1 + S_2 ex (9^5) to an endpulse input on Panel 10 (10^3) and then sending a single (D18) "1" into 10^4. The pulse circulated but soon dropped out. The sensitivity of f_1 set was increased by inserting 150 ohms in cathode of V_2 panel 9 & this made everything quite stable
The W_{12} & W_{13} flipflops were then tested by putting D_0 onto 10^1 (the R_1 + R_2 input of Panel 10) in addition to the circulating pulse causing W_{12} & W_{13} to operate at half minorcycle repetition frequency

This worked satisfactorily first time but on removing the circulating D_{18} the W_{12} & W_{13} reverted to operation on a minorcycle frequency. This was found to be due to

sensitivity ~~of~~ to pickup on the mechanical EP line 10^2 as on earthing this input the W12/13 waveform ceased.
An extension of the feedback loop was then made by feeding a single D_0 into one of the endpulse lines (10^4) & taking the resulting S_1+[S_2] from 12^1 & feeding this back into R_1 + R_2 (10^1) to start stage 2. ~~A~~ D_0 was fed to 12^5 to give an output from 12^{12} which was fed back into an EP line. After triggering the flipflops to correct

[[NB03-024]]
condition for a start this worked well from a single shot.

16-8-50

Coincidence units connected up to Coordinator units & circulation achieved by feeding back. No adjustments were required other than to kick flip flops into correct startup condition. Standard wiring was used with exception that D_0 fed to 12^5 and 12^{12} fed to 10^6. This gave a 3 minorcycle circulation after being stimulated by a single D_0 on 10^3
Coincidence waveforms normally ½ m/c could be lengthened by

simulating F1- with a crock clip to earth.
The circulation could be conveniently stopped by putting a negative waveform from the single pulse generator onto the Inhibit endpulse line.
A start was made today on Action Static registers & decoders with a view to producing correct coder waveforms from the binary form of the orders as simulated on the number simulator. The static registers were found to be working correctly but on operating on them from the number simulator and

[[NB03-025]]
triggering off the Prim Action Decoder from the circulation of pulses in the main coordinator Control & Coincidence loops it was found that the output from the Prim. A.D. had some signs of breakthro. This is probably due to the rate at which it is being triggered and it is probable that it will be necessary to use the slow speed of the single pulse generator.
Under working conditions the static registers will be set repeatedly at minorcycle repetition rate but there willl not be an output from the P.A.D. until S^1 sets

its flipflop. The output from the PAD will then persist until a reset pulse is received at the conclusion of stage 2 of the Coord sequence.
A more natural sequence to use would be :-
(1) EP from Single pulse generator
(2) ~~Order~~ SCT to Coord [[ex]] ~~prim A dec~~ number simulator having only action digits i.e. 0000 as address. This will give earliest possible coince if ~~sequence control~~ counter input is also 0000
(3)

[[NB03-026]]
Mods to Coord etc
Panel 9. transfer grid V_4 to other side of D_1. ie cathode V_{3A}

17-8-50

In testing the Primary action decoder the following apparently fundamental difficulty arises. The ~~S_2~~ R_2 end pulse resets both the static registers and the P.A. flip flop at the same time.

~~In the case where a negative waveform has been set but a corresponding positive waveform~~
In the case where a gate is fed with (a) two negative waveforms ~~(b) a positive waveform and (c)~~ & b the P.A. waveform, and ~~the~~ one negative

waveform is in the set condition (ie earth) while the other remains reset then the following waveforms are applied to the gate:-

[[diagram]]

This could apparently be overcome by delaying the reset to Action SRs by 1μS
It has been agreed that such a delay should be included.

[[NB03-027]]

17-8-50 pm.

Further progress has now been made, all decoders appear to be working satisfactorily from appropriate SRs Tomorrow we move on to the coder so that the desired combination in an order will produce the appropriate order waveforms. Having done this we will ~~move~~ commence work on the counter tank so that the length of circulation loop can be lengthened by the time taken to find coincide[[nce]]

18-8-50

In testing the coder it was found that the switching of the number simulator was at times causing the circulation in the Coordinator loop to stop. It was found that at the same time that this happened the ff_1 in Coord Control I~~X~~ was not being <u>reset</u> by a D_0 and was remaining in a jammed condition. ~~It w~~ The connection between this and the number simulator switching was not traced but on making f_1 more sensitive the trouble ceased.

[[NB03-028]]

<u>21-8-50</u>

A good deal of today was spent in getting a certificate to drive a Lyons private car. On the machine the Coder was proved to be functioning satisfactorily and we then went on to the counter tank. This did not work at first and after a little chasing found that the dividing circuits had slipped back to counting 35. This has not happened for some time but it is a fault that will have to be cleared eventually.
With the counter tank counting inspection of the coincidence

waveform showed that it was correctly giving a half minorcycle coincidence gate once every 16 minorcycles ie when the counter tank found coincidence with zero.

<u>22 8-50</u>

Continuing tests on Coincidence unit numbers were set up on number simulator and used as OT output. It was demonstrable that the timing of the Coincidence waveform was dependant upon the configuration of the number set up. ~~One trouble was that~~
A fault shown up here was that

[[NB03-029]]
D_{25} in the number had the effect of preventing coincidences but this was eliminated by reducing the delay d_1 in panel 45 which had been letting sufficient of D_{25} thro to produce an anticoince pulse.

A second problem was that a D_{20} in the number simulator was ~~causing lack of~~ inhibiting completely coincidence waveform. This is correct as the D_{20} corresponds to the least sig digit of the even half minorcycle and should be a zero. The coincidence unit was trying to find coincidences with an even no during the odd half and an odd no during the even half

and consequently failed.

23-8-50,

Sequence Control tank now functioning but no effort yet made to transfer from Order tank (number simulator) to SCT. This should be next step.
Shaw is making good progress with Raster scope. It seems likely that we shall have an excellent representation of 1s & 0's from this

[[NB03-030]]
Parts & Processes still to be tested
(a) ~~Conditional transfer.~~
(b) Transfer Units + Tank.
(c) Tank No SRs & Decoders.
(d) Store
(e) Order Tank
(f) Long Short Discriminant
(g) Computor Processes from Programme
(h) Input + Output.

24-8-50

Conditional Transfer operated by single pulses as D_9. Order Tank filled & working. Single long tank connected up & filled with clock pulses, Counter tank operating at same time i.e. frequency satisfied both long & short tanks. This latter test was not conclusive as no tests were made on computor tanks at the same time.

[[NB03-031]]

25-8-50

No great advance today
Some time spent preparing the way for the use of store ie connecting up Decoders & SRs but more spent on assistance to Caminer & Shaw.
Raster scope seems to be sensitive to amplitude of synch pulses & may have to have separate synch controls for line & frame.
Caminer's work on frequency control of clock pulses has been hindered by spurious frequency modulation of clock pulse oscillation

Future programme for Coord & Store Tests.
1. Ensure that coince waveform is getting to Rack "0"
2. See that C17± is giving one coince each to output and input & clear gate of selected panel 1.
~~3. Use A & T orders to~~
3. Use SPG to inject number simulator setup into order tank ~~and~~ (I_0, I_1, I_2, etc)
4. Use SPG to single step Orders inputting number simulator into consecutive store positions store must be clear to start with & order tank clearing must be inhibited

[[NB03-032]]

28-8-50

By eliminating secondary tank N_1 decoders it was possible to operate output gate of a panel 1 in the store. Then, by reversing C17 leads the Input & clear ~~waveform~~ gates were operated. Then by connecting feed line to number simulator an attempt was made to transfer numbers into the store.
Here we met trouble. In order to compensate for the fact that the number simulator only has minorcycle repetition whereas the order tank gives ½m/c repetition

the coincidence waveform was made a 1 minorcycle duration by tying down the valve taking F_1- to earth.
Then by stimulating the Coordinator with a single pulse from S.P.G. the number set up was transferred into the store. This worked for positions 0 & 1 but not for position 2 or 4 or 6 etc
all odd positions working correctly. This may be due to bad logic in setting up our tests.

[[NB03-033]]

Contents of SCT	Counter	Coince
0000		
0000	0000	000x
0000		
0001	0001	0010
0000		
	0010	
	0011	
	0100	
	0101	
	0110	
	0111	
	1000	

This is apparently due to the fact that the number [[ex]] the number simulator is only present in the second half (odd half) of the minorcycle

Explanation
(a) When ~~but~~ first end pulse is sent SCT is clear & coincidence is found with compartment "0". This means that coinc unit has compared digits D_2 to D_6 of counter tank & SCT & found them agreeing. The consequent coincidence waveform starts at D_{18} of same m/c & finishes at D_0.
As the digits of the number being transferred are in the latter half of the minorcycle it appears to be transferred intact.
(b) When the second end pulse is sent coincidence is found with 0001 in the SCT and this time coincidence waveform is set up at D_0 and owing to the fact that the effect of [[F]]1 has been inhibited it lasts for a minorc[[ycle]]

[[NB03-034]]
The number therefore appears to go into the second half of the second minorcycle compartment of the store.
(c) The third end pulse causes coincidence with 0010 but as in case (a) the coincidence waveform starts at D_{18} & finished at D_0 and the digits of the number

transferred are superimposed over those due to (b) If the same number is being transferred as in todays check then there will be no change in the contents of the store.
Similarly new numbers will be entered for end pulses four six & eight etc but those for five seven & nine will be

super imposed on the number entered by the previous sequence.
This error into which we have fallen in testing the Coordinator is one which the programmers will have to avoid ie long numbers cannot be transferred into compartments having an even address.
This argument may be proven by altering the number & seeing that the resultant in the store is right for the first end pulse but a mixture of each pair of subsequent numbers for each pair of subsequent end pulses.

[[NB03-035]]

29-8-50

Yesterdays theory has been tested & proved correct, different numbers have been put into all the store positions in one tank and when new numbers are put in, irrespective of ~~the~~ whether they correspond to odd or even nos in the SCT they are superimpos[[ed]] on the previous no. On connecting up a negative coder line to the clear gate the previous number was replaced by the new one.
The next step is to include in the feed line the Transfer tanks so that numbers can be fed from the no simulator into <u>either</u> half

of the minorcycle.
Two tanks were made up this afternoon - the last of our stock - the old ridged washers being used rather than have to wait for the new washers due next Friday.
Shaw has temporarily left the Raster Scope in order to concentrate on the Transfer Unit which is now nearly tested. After this he will test a new Static Register for ½ cycle + L/S discriminant before returning to the Raster Scope. In the meantime we can make do with a

[[NB03-035a]]
[[as previous image, but darker]]

[[NB03-036]]
spare half of a SR operating for the ½ cycle F_2 only L

30-8-50

New block schematics are required for notebooks.
(a) Complete Computer & Coord.
(b) Coord & Coince

<u>30-8-50</u>

Transfer unit & tanks now available also the raster scope in a temporary form.
<u>But</u> still having trouble in getting numbers into both halves of the minorcycle in the store.
After many false starts the trouble has been resolved in part as although the number is arriving at the store in the correct half of the minorcycle ie the transfer tanks are working, the coincidence waveform is arriving some minorcycles before (or after) the number starts (or finishes) from the transfer tank. Now this fault will only be

[[NB03-036a]]
[[as previous image, but darker]]

[[NB03-037]]
apparant for one half of the m/c as in the case where only ½ m/c delay is required the input gate ~~has to be opened~~ is normally open and the F_1 or F_2 waveform on being set, shuts it.
In the other case 1m/c delay the input gate is opened by F_1 or F_2+ Now it is obvious that the F_2 waveform is not up at the same time as the coincidence waveform
Now the setting of the Static registers is done by the number ex Sequence Control Tank or the order tank being gated against W_{13} or W_{12} respect

It is possible that for some reason coincidence is only being found in the stage II ~~and~~ when there is no order digits to set F_2. ~~On second thought this cannot be the case as in stage II the ouput gate of the store would be chosen by C_{17}~~
Points.
(a) SCT no is setting F_2 as proved by no getting correct delay in Transfer
(b) This suggests that it is the Coincidence waveform that is wrong
(c) Should there not be two coincidence waveforms ie one for each stage? In fact one

[[NB03-038]]
only is observed & this may be coincidence with 0000 in the order tank in stage II which should not be accompanied by an F_2 waveform.
d Obviously the facts to check are whether the W_{12} waveform corresponds with a coincidence waveform & then ~~to~~ if not to investigate the reason which is probably in Coincidence Unit.

31-8-50
It seems today that we have made negative progress in tests on the coordinator. In the first case we seem to have reached a state now when all the key pulses happen too infrequently to be seen on the C.R.O
As reported yesterday it is possible at present to put numbers into the store only in the less significant half and when it is attempted to put them in the other half the coincidence waveform just doesnt correspond in time with the no's going to the input gate. When the coince waveform is compared

[[NB03-039]]
with ~~the~~ W_{12} W_{13} ~~wav~~ it appears correctly placed (incidentally I must compare W_{12} with F_2)
To add to our troubles an inadvertant HT short burned out ~~the~~ a cathode load in a DPGen, a subsequent stray piece of solder caused a small fire in the C.PGen and on resuming work on the racks, it took about ½hr to find an HT fuse blown in spite of a brightly glowing neon which was taking its current from the negative line!

[[circuit diagram]]

Programme
(a) Counter Tank Working

(b) SPG to EP line
(c) Compare W_{12} & Coince Wave.
(d) Compare W_{12} & F_2 every second sequence
(Raster scope should be by Coord Racks for ease of working)

[[NB03-040]]
Possible future testing assuming satisfactory control by coordinator
(a) Clear SCT & Hold Order tank clear.
(b) Single end pulses to Coord from SPG.
(c) Output of number simulator to discharge line (Input)
(d) Reverse C17±
(e) Set up [[Series]] orders and data on number simulator and inject into store by ~~push button~~ single pulse from SPG for each order/number
(f) When all orders & data are stored remove clear from order tank revert C17 ~~&~~ clear SCT, & reset W_{13}

(g) remove number simulator from discharge line
(h) Single pulse from SPG to Coord to start sequence
(i) Inspect results in store and computer registers.

One Knotty problem which is not very easily solved, showed up on one occasion when the adding of "1"'s into the SCT was inhibited so that the effect of repetitive end pulses could be more easily examined. The number which had been set up on the no simulator should of course have been continually

[[NB03-041]]
transferred into the same position in the store. Instead of this it appeared after a lapse of a few seconds in five positions one ~~of~~ being filled after another in a fairly random fashion.
It was always five positions and the relation between these positions was always the same ie. the less significant halves of minorcycles 1, 2, 4, 8 & 16, thus :-

[[diagram]]

The number in the sequence control tank during this test remained at "1" and when the[[~~re~~]] contents of the SCT & the Counter Tank were compared on the same CRO there was no apparent shifting of either number. Coincidence was apparently being found between numbers as follows:-

SCT	Counter Tank
00001	00001
00001	00010
00001	00100
00001	01000
00001	10000

[[NB03-042]]
The only ~~two~~ three reasons for such a behaviour of the Coince circuits seems to be
(a) One of the two numbers is being subject to shifting.
(b) Some delay in the Coincidence waveform of [[c definite]] number of minorcycles.
(c) Counter tank not counting correctly

1-9-50

Coord & Coince circuit

With a single 1 in the SCT and further "1's suppressed repetitions of end pulses showed that coincidence was occurring in compartments 0 1 2 4 8 ~~as~~ in a random fashion but none of these corresponded to a time when the number in the number simulator was available

Comparing F_2 with coincidence waveform under these conditions

---- very difficult to see but coincidence might be happening in the last half m/c of the F_2 or in the first half after F_2

[[NB03-043]]

~~Remo~~

Examination of the input number into the store showed the pulse pattern coming up in alternate minorcycles (Raster) By removing the input to transfer tank II [[I ensured]] that only the F_2+ opened path was available & checked that the input to the store was now in the more significant half of the minorcycle (1 m/c delay in the transfer tank).

Now comparing the number input to the store and the coincidence waveform showed that the coincidence waveform

was happening an appreciable time after the number appeared.

Comparing the number into the store and the F_2 waveform it was seen that the number disappeared long before the F_2 waveform finished.

This was apparently due to the very long time that F_2 was up as shorting out the input capacitor on the input gate of the Transfer I ~~removed any~~ allowed the number to go in.

This suggests that the real trouble is the long line between stimmulating Coord and the Coincidence Waveform.

[[NB03-044]]

The obvious course to follow is to question why the coince was taking so long to find coince.

Checking up on anticoince pulse ex 45^{10} on raster scope there was a constantly changing pattern ~~possibly~~ due to the W_{12} waveform going up & down and interrupting SCT total going to coincidence unit. By passing 12^6 to 12^{10} the anti coince pattern became stationery ~~with coince~~ and it was noticed that the F_2 & W_{12} waveforms were more normal. With this setup it was possible to transfer numbers into

correct positions in the store after permitting SCT to count once again!

This suggested that the reason for delay in coincidence was ~~the SCT in~~ somewhere to be found in panel 12. It transpires that the coince unit was unable to find coincidence at all with the SCT total as emitted by panel 12 and only after the charge on the condenser coupling from W_{12} had fallen to such an extent that the gate was closed again and the SCT total was prevented from going out, did the

[[NB03-045]]

coincidence unit find coincidence - with zero.

Inspection of the output from Panel 12 suggests that the reason for non coincidence was the disimilarity in shape of the pulses presented to the coincidence seeking

circuit. I feel that this call for a balancing control on the CU before reliable coincidence can be expected.
By reducing amplitude of Panel 12 output a fairly accurate transfer of numbers to the store can now be obtained.

After establishing that the necessary orders could be reliably stored in the desired store positions, the orders & data for the first of a series of simple programs were put into the store. A brief effort to make the computer work was made but apart from establishing that a number could still circulate in the accumulator no progress was made. One fault to be followed up on Monday (provided that the injection of orders is still working correctly) is that the

[[NB03-046]]
orders do not appear to be circulating in the Order Tank. This may be due to certain disconnection that were made during previous work on the computer.
---
500 yards of coaxial sent to WK.
Cosford to phone re oscillator part for new frequency control.
Stores to be collected.
B.F.O. Returned to C&G College

4-9-50

Work today is likely to be interrupted as an electrician will be ripping up floors to do Rack bonding. There are several jobs which can be done during this enforced shutdown.
(a) Clean up Raster Scope
(b) Check wiring of coordinator for normal working with computor
(c) Arrange for electrical switching of C17±
(d) Insert balancing controls in Coincidence seeking circuit.
(e) General check up on Computer.

[[NB03-047]]

[[diagram]]

100K HS 1W
2x 5K HS 1W
1x 10K HS 1W
20K Pot
2x 1 Meg.
3x 330Ω
2x 2K2 5%
1x 3K3 5%
2x .001
2x 0.1

6-9-50

While bonding of racks has held up progress on computor a little thought has gone into reciprocation.
It now seems that the following mods will be necessary

1. New Coder C_x representing Recip
2. Coder C_y (C_x + C_4) used in 26 to stimulate sequence with S_q
3. Coder C_z (C_x + C_5) to ~~give~~ open TCT gates.
4. D_y, D_1 & C_x gated to give $1D_1$ which is mixed as on AD1 in Acc10.
5. W_5, W_1, Mier A [[link]] gated to give number to be added or subtracted from Acc 6

[[NB03-048]]
1_1 7-9-50
Work on Coordinator Continued. The amplifier inserted in the Counter Tank / Coincidence lead has improved matters considerably but although reliable coincidence is being found now the settings of the two controls (a) amp of counter tank output, (b) amp of SCT/OT output, are too critically interdependant for a permanent arrangement. It seems that the only safe way to deal with this is to delay and clock both inputs before presenting to the coincidence seeking circuit.
Having achieved correct coincidence I moved on

to the first programme but found no success here as no end pulses were being received from the computer.
Investigation showed first of all that the correct coder waveforms were not being set up. This was traced to static register LC7/4 where a 62K High Stab resistor had gone O/C. This produced the coder waveform OK but still no end pulse from computer. Neither is any number being transferred into the computer in response to the A order. This latter

[[NB03-049]]
point has been found to be due to ~~inter~~ the input output leads to the computer having been reversed.

The Standard Telephone Team have been working here this week with the first tape m/c. Tests here have not been too satisfactory

---

Lifting tackle for the batteries is now fixed and tested to lift 1 ton.

Shaw is working on Pulse selector units and these seem to be

~~8-9-50~~

proving reasonably satisfactory given minor modification. Cam has nearly completed the frequency control units which should be capable of holding the frequency to within about .01%

8-9-50

Continued work on the Coordinator has produced more headaches. The present fault defying solution is the lack of coincidence in stage II. I have not felt very bright today & there is a singular lack of ideas maybe a weekend of rest will help.

[[NB03-050]]
Mr Simmons was shown the Raster scope this afternoon & was very impressed with the way numbers can be put into the store. I fear he went away feeling that the m/c was almost complete but personally I see a lot more troubles aheed before we dare give a second demonstration.

Hemy has been agitating re reciprocation so I have worked out a scheme pretty thoroughly now which will fill the bill. It will involve quite a number of additional

mixers & gates, but should be worth the trouble from the programmers point of view. It has occurred to me that money values will be saved in such a mod, and may ~~be~~ even be eliminated from the machine by combining our mixer system with the line terminal idea. eg. If three outputs from three different panels ~~are~~ have cathode follower outputs and the CI^5s have .10K load each there seems to be every advantage in taking all three lines to a common resistance on the receiving panel thus serving

[[NB03-051]]
the three purposes
(a) mixing
(b) terminating
(c) eliminating input cathode followers.

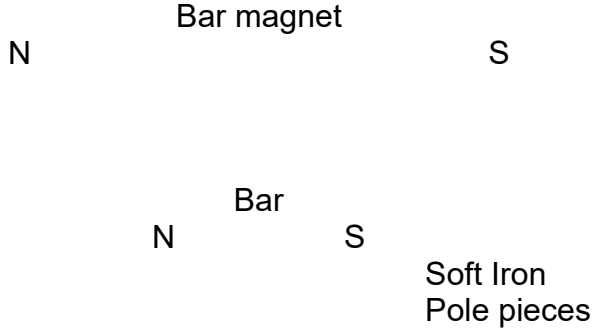
[[diagram]]

[[diagram]]

In most cases a cathode follower will be required to give the correct voltage level on the ~~input~~ receiving unit but in some cases this may be dispensed with

[[NB03-052]]
Moving coil pickup

[[diagram]]



11-9-50

Review of Progress.

Machine (a) Coordinator not yet working with Computer
(b) Mod needed for C.S.C.
(c) Underfloor Bonding complete
(d) but overhead waiting for braiding
(e) Frequency Control unit nearly ready for trial
(f) No check yet on length of tanks
(g) Shortage of SRs & Decoders prevents more than one storage tube being used.
(h) ~~T~~ Order Tank phase.
Testing After Pulse Selector Units have been finished, need for remaining SRs &

Decoders.

[[NB03-053]]
Required - circuit checking.
Can Dutton be used for this.
Workshop Generally
Lifting Tackle fitted & tested
Required Lab-boy.
Cossor CRO ~~at~~ in dock.
Drawing & Office Work for Miss P.
Store check.
Valve Numbering
Components (faulty) Register
Vaults
Elct drawing office working on Heaters.

Work on Machine

Continue check on coordinator. Get "add" into every compartment of store & set on repeat. Then chase thro coders etc into computer.

After chasing coders thro computer it was discovered that end pulses were being produced but not passed on by CC U VI. This was due to a fuse having blown in this unit.
On rectifying this and with a store full of the "add" order a single pulse produced ~~an~~ a long sequence of adds but after 256 "1"s had been added into the SCT it stopped. This was due to the

[[NB03-054]]
fact that ~~only~~ after that number had been counted the Tank No SRs had switched the coincidence waveform to ~~be~~ Rack 1. ie only 8x32 = 256 store positions available on rack 0. It was not considered worth while to alter this arrangement although at some future date it may be desirable to make this add sequence circulate indefinitely by inhibiting the switch to other racks.
It had been noted that no number was being added into the accumulator and this was soon found to be due

to the multiplicand tank which ~~req~~ had been put out of adjustment by the insertion of a new attenuator screw.
At this stage all the short tanks of the computer were lined up (attenuator screws & gain control) before continuing. Programme I was now tried again without success so a return was made to fitting the store with Add (note digits 19, 33, 34, 35, the 19 being used to observe effect of adding this order into the accumulator.) Here an unexpected trouble.

[[NB03-055]]
arose as the "1" put in to indicate addition in the accumulator turned out to be in the right position for dealing with long numbers so that the number added instead of being 11100---01 was 1110001011100---01.
This was put right by making the "1" a D_{21} which placed it well into the address part

of the order (note I must be sure that it is not in a position that will transfer a number from a tank that doesnot exist!)
According to my [[recogning]] this should have put a 1 into

the accumulator for every 1 added into the SCT but here all was not well as the number put into the accumulator changed for each try.
At this stage a ~~list of~~ programme of procedure was written down as with all the clearing & reclearing of the OT & SCT etc etc ~~the~~ it is becoming increasingly easy to forget a vital step thus making a whole sequence meaningless.
At this stage also something went wrong with the coord as "1" were not added into SCT for each push of the button

[[NB03-056]]
although a check was made on the condition of the various flip flops.
At the time of shutting down this evening there seemed to be some relation between the number put into the store and the fact that the SCT did not get its "1"s
I am finding it increasingly difficult to pick up my train of thought ~~due~~ after to the several interruptions that inevitably occur.
TRT & JMMP returned from holiday today. I set LEO LEO up in lights on the raster scope for their

benefit and they were duly impressed.
One of the 339 cossors has developed a fault on the T.B. This means that we now have 3 scopes out of action a state of affairs which must be rectified

[[NB03-057]]

Experiment to Try Out.

If a panel I has its clocking gate held open, and clock pulses fed into it for more than ~~the~~ 16 minorcycles then the pulses returning from the tank (assume a long tank) should be in phase with those leaving. If the delay in the tank alters (e.g. due to temperature) then the phase of those arriving will be slightly different from those leaving ie if it takes longer to get around then the frequency of the pulses leaving will begin to become less I.e. the set up should become similar to a self sustaining

oscillator whose frequency is controlled by the time delay of the tank.
If now, as seems reasonable to suppose, the waveform at any particular part of the circuit becomes sinusoidal, then it would appear that such a set up could be used as an oscillator to produce clock pulses whose frequency would be controlled by the time delay of one tank. The abnormal requirement of such an oscillator would be a stand by oscillator to produce the original train of clock pulses to start the circulation.

[[NB03-058]]

12-9-50

A satisfactory answer to yesterday problem has not been found. although quite a bit of progress has been made today. It appears that the amplitude of the SPG may not have been sufficient to do the necessary setting & resetting of ff as after a small adjustment this was behaving more normally this morning. The first step today (assisted by Shaw) was to get "add" into every compartment of the store whereupon the first push of the button produced the required 256 "1"s into the SCT.

An attempt to put a digit in with the A order so that the effect on the accumulator could be studied was not so easy as at first appeared as the extra digit according to its position caused different effects when treated as part of an order.
In order to make the effects of the order easier to inspect I removed the SCT line from the Tank No SRs F_{10} + F_{11} so that now the repetition could go on indefinitely which in fact it did so that the SCT gave the usual half adder

[[NB03-059]]
picture. This showed that the "A" was in fact going along the correct channels and in fact being added into the accumulator although the correct working of the latter could not be vouched for.
The next experiment was of course programme I again. Again no luck.
Then I decided to try an indefinite repetition of the programme by ~~preventing~~ inhibiting "1" from SCT. This was not immediately succesful and adjustment to the CSC had to be made before a

stable pattern of coincidence waveforms could be seen.
Eventually however a satisfactory condition was obtained and the number seemed to be added into the acc correctly but of course no real check could be made owing to the speed at which the numbers were being added.
A return to Programme I at this stage still gave no results until by accident (or despair) after pushing the button once I continued until ~~the~~ coincidence was bound with the first order again

[[NB03-060]]
Lo & behold the number went into the accumulator.
This was repeated several times and there was no doubt that if the machine was allowed to select each compartment inturn as an order, it did, when it got round to compartment 0, carry out the programme as designed.
One new puzzling thing about this was that the number having got itself into the accumulator promptly got itself cleared again at the next push of the button.
It appeared that the next compartment containing the order

D_A 20 21 22
1 1 1 1 - somehow called for the accumulator to be cleared!
This difficulty was bypassed by making the number up of D21-24 and with this set up the number 1111 was left in the accumulator and added to next time round.
This was allowed to repeat a good many times to see that the acc was functioning correctly only to find that it was <u>not</u> early signs of a leaking crystal are visible, and only after bringing the gain controls up considerably was I able to repeat the addition of 1111 up to ~~124~~ 128 times without error

[[NB03-061]]
The problem that is left to be solved is - why will this programme not work with a single push of the button when it <u>will</u> work after a number of pushes. The answer to this is probably in our method of setting up conditions for a start. Perhaps a D_9 would work when a EP would not. I must investigate further!

~~<u>Possible reasons for a non start</u>~~
~~<u>When</u>~~

Present method used for starting program - (which is not successful)
(a) Assume program of orders in store position 0 1 & 2
(b) Clear SCT
(c) Reset W13
(d) End pulse sent to Coord.
The result of this is that the first order gets into the OT but apparently is not carried out ie error occurs in stage II
This suggests that the W13 flip flop is not getting set by $R_1 + R_2$ It is possible that this f is slightly unbalanced and needs more than 1 kick to send it open

[[NB03-062]]
after it has been in the reset state for some time.

13-9-50

Examination of the W_{13} & W_{12} waveforms under repeated conditions showed that ~~occal~~ occasionally W_{13} was not being set (its normal position while waiting for the next EP is set). To cure this it was made more sensitive to set pulses by increasing cathode load by 100Ω
Returning now to Programme I with no success, working spasmodically only after

going thro a complete cycle of 32 pushes on the button.
At this stage it was decided to investigate the size of pulses going to set & reset the various ffs in stage 1 & 2. In order to see these infrequent pulses the raster scope was pressed into service by removing the frame time base value & applying the pulse ~~direct~~ via a condenser to ~~the~~ one Y plate. With this set up single pulses could be seen fairly well.
Only on the set of W_{12} was there any doubts where there appeared to be a double

[[NB03-063]]
pulse :- [[pulse diagram]] This eventually proved to be ~~the~~ caused by the differentiated version of the waveform of W_{12}.
~~One thing that required~~
Returning again to the programme it was found impossible to put the orders into the correct position in the store as at the first EP a 1 went into the SCT inspite of the fact that the W_{13} had been reset.
After a good deal of investigation it was concluded that the differentiated version of the W_{12} waveform was emerging via

the reset input and causing the now extra sensitive W_{13} to set with the first EP so that the R_1+R_2 pulse from the Coord was able to pass via panel 11 to the SCT. This would also have explained the double pulses which were seen to be added into the SCT on some [[occasions]].

[[NB03-064]]

14-9-50

This morning, reduced W13 to its original sensitivity (it now has 220Ω extra in each cathode) On slow repetition W13 compared with W12 W13 fails to set about once in 50. - there is always a W12 waveform at the time W13 fails.
After trying for some time to correct this without success it was decided to realign the setting & reset sensitivity from scratch. This resulted in each ff having 220Ω in each

cathode and being approx equal in

sensitivity probably about 12 volts.
Returning to a repetition of "add" everything seemed to be work OK but once again it was not possible to do programme I from a single end pulse. If a D_9 was used however it worked sometimes but accumulator was not accepting number.
A further check on the repetition of add was successful in chasing the number thro into the accumulator but when a return was made to the simple programme the SCT refused to accept "1"s

[[NB03-065]]

15-9-50.

Refusal of SCT to accept "1"s
Possible causes :-
(a) Half Adder not functioning
(b) End pulses too small (Amp on P_{11})
(c) Tank & Panel 1
(d) R_1+R_2 failing to set ~~f3~~ W_{13} (see facing note)
(e) Single Pulse generator not working

During yesterdays work it was decided to separate the set of W_{12} from the reset of W_{13}. This was done by using a spare half triode on another panel. It did not however have the desired effect and the theory that the differentiated form of W_{12} going up was setting W_{13} is now in question.
On the other hand an investigation of the behaviour of the gate letting the R_1+R_2 thro to set & reset would be worth while as if there is a breakthro of the W_{12} gateing waveform as it goes up this might be sufficient to set W_{13}. If this happened R_1+R_2 would try to set & reset W_{13} at the same time

[[NB03-066]]

15-9-50

Some progress to report. The W_{13} waveform had been noticed to take a long time to reset under slow repetition. On close examination it was found to be taking 10 minorcycles.
On slow repetition the condenser coupling to panel 12 has time to ~~decay~~ discharge & therefore the waveform ~~when reset~~ when reset takes the input grid well below earth. As the grid is restored to +10v this means that ~~the~~ until this input condenser can be recharged the cathode follower has a virtual short circuit across its output. This was overcome

*

by treating the waveform as a negative going one & restoring to +40 volts.
Later. Programme 1 has been done repetitively ~~but~~ i.e. by stepping SCT on thro more than 32 steps but still stalls on simple E pulse operation.
It was found that W_6 was occurring much more frequently than required infact every R_2 pulse produced W_6 irrespective of the order. This was due to a spike on the Coder 1. On inserting the delay in the ASR reset as agreed some time ago the spike was removed from the damper area.

[[NB03-067]]

It would be desirable however for this flip flop to be a little less sensitive.

18-9-50

A great step forward today with all four of our first test programmes successfully carried out.
A good reason has been found for the fact that a single end pulse was not successful in carrying out any programs. In order that the coordinator should call out the first order from position 0 of the store it was necessary that W_{13} should be in the reset state so that a "1" was not added into the SCT initially. Now the W_{13} waveform as reported previously

was AC coupled to panel 12 and owing to the fact that it had to stay in the set state for long~~er~~ periods it was necessary to treat it as a negative waveform. Now in resetting it at the start of a programme had the same ill effects as had been experienced before when it was used on slow repetition.
As this is a wholly artificial state of affairs it was merely necessary to use a single D_9 instead of an End Pulse to start the sequence . as will happen in the starter sequence.
From this stage it was

[[NB03-068]]
easy to do programmes 1 & 2 consisting of Adds into the accumulator. Programme 3 entailed transferring out of the accumulator to the store and this failed.
Tests showed that there was no input waveform to the store and this was soon traced to W_{17}+ which had a long tail Two errors in wiring in the coder accounted for this ie no +50v to grid of V and zero restoration inversed or V
When this was corrected programmes 3 & 4 were

carried out successfully.
It is felt that todays progress brings us within striking distance of our target date of Xmas, provided that the starter unit can be produced in good time.
If there is likely to be any serious hold up on the starter it will probably pay us to make up a bread [[board]] of the starter
Hemy is joining us tomorrow to make up some more program[[mes]] so that more computer sequences can be put to the test.

[[NB03-069]]
Add -- Short -- Long
Transfer T Short-- Long
" U " "
Shift L " "
Shift R. ' "
Collate
Mult
Subtract
Repeat all above sequences with negative numbers.
Programs required that ~~will~~ can be extended without removal of first orders.

Temporary
Extensions to machine to assist testing.
(a) Relay & Lamp to indicate stop

(b) " " " overload
(c) modified starter unit to give initial orders.

[[NB03-070]]

19-9-50

More progress today followed by a decision to halt for some modifications.
After some discussion with Hemy & Caminer this morning H produced two programmes to test the E & G orders.
These gave an amusing picture as it was arranged for 1s to be added continuously into the accumulator until the total carried into the sign digit. Both of these programmes worked OK although a fault caused some trouble in getting the orders into the store at first

This fault was found to be due to the fact that no provision is made for mixing the discharge lines from the In/Out and the Computor. As the pulses were of different amplitudes & terminat[[ed]] differently the amplitude control in the Transfer unit is not the same for both conditions It has been decided to put a new mixer on the transfer unit to accommodate the I/O numbers.
A second fault that requires investigating before further work is done on programmes is ~~the~~ causing

[[NB03-071]]
W_{12} waveform to get stuck in the set state so that it has to be kicked over Before a sequence can be started. Once over it behaves ok but when needed again at a later date it is found in the set state again.

20-9-50

A reconsideration of the Reciproc[[ation]] sequence including an examination of the mathematical principle involved has led to a conclusion that the same process could easily be turned into a division process.
The process described earlier of continued subtraction or addition of the denominator to a single 1 is nothing more than dividing the denominator into 1 by the Myers method. If the same process was used to perform the same operation on a different numerator, then the only difficulty in the way of obtaining the correct answer is the fact that the

[[NB03-072]]
the ~~numerator~~ denominator must needs be bigger than the ~~den~~ numerator in order to ensure that the ~~fi~~ answer to the first subtraction is negative.
At first glance it would appear that the programme staff might jump at the opportunity to whittle the time of a division down to the equivalent of a multiplication, but the reverse is the case. In order to ensure a correct answer to a division sequence they may have to shift both numerator and denominator ~~and then~~ and might even need to inspect the size of the number being divided. This involves

complication of programmes & a possibility of more store space for orders.
I feel that probably the best course to take is to make it a division process with the option of dividing into 1 or any other numerator left to the programmer. It remains for the programmer to decide where he wants the answer. If it is left in the Mier tank it will need two orders to get it to the store whereas if it ~~remains~~ is put in the

accumulator (not an easy thing) then he will only need one, but will not

[[NB03-073]]
be able to multiply directly if the result is a reciprocal.
In order to make the R_n process a division process all that is required is to inhibit the first 1 into the accumulator (a simplification as it does away with a gate & some mixers)
The D process should be stimulated by the first digit of the denominator as in Mult.

Price of Stools ex Joiners
2 more steel stools
3 - bentwood chairs.

Miss Cox re stock control.
? Wayne Kerr Stock

Valves	Valve No	Date
	3r2	9/50

[[NB03-074]]

20-9-50

~~be able to multiply directly if the result is a reciprocal~~
The dissimilarity between ~~num~~ amplitude of digits coming from number simulator & the computer has been removed by putting a new mixer in the transfer unit. The number simulator had had an unfair advantage in that it was being supplied with clock I This has now been rectified.
A new attempt on programme 7 was not wholly successful and it appeared to fail on the G order. This caused us to return to Programmes 5 & 6

Programme 5 worked OK but 6 stalled on the G order. An attempt to do a series of G orders was frustrated by a series of faults which all seemed to arise at once and all of which have not yet been traced.
(a) Add order refused to produce W_6 but this was intermittent and would not go wrong again
(b) F_{16} appeared extra sensitive on reset and this SR had to be replaced.
(c) F_1 started to operate in stage 1 causing number & orders to go into both halves of the

[[NB03-075]]
minorcycle. This is apparently being caused by a D_{19} appearing in the total of the sequence control tank. The source of this pulse has not yet been traced.

21-9-50

There must been some bad observations which led to conclusion (c) mentioned above. In fact the input gates of both Transfer Tanks 1 & 2 were going up but at different times probably operated by F_2. The cause of the extra D_{19} in the transfer tank is a comparatively simple one. The Static Register

which was used to replace the A S R producing F_{16} had not been tested and in fact it was causing the trouble by producing an Input order (F_{16}.) thus providing a

[[coincidencing]] waveform in Stage 2 (by setting up C_{25}) This produced a second R_1+R_2 from coincidence unit which in turn produced a second 1 to S.C.T. By the time this fault had been located, Shaw had fixed the original SR (two faults on this (a) a grid resistor missing and (b) an off-value H S resistor.)

[[NB03-076]]
After re-installing the original S.R. I went back to the G programme with no luck. Then back to E programme which worked spasmodically, occasionally sticking at the E order.
Mr Thompson, back from a Programming course at Cambridge saw the programme carried out & immediately asked the possibility of a demonstration. I told [[him]] I thought the machine was too uncertain as yet to warrent this.
Caminer had ~~finished~~ brought the frequency control unit to a stage which warrented a try out. This we did, but

had to make one or two adjustments to CPG to give real control. After these had been made & it seemed to be working satisfactorily we switched on the heat in the vaults to see what control there was in temperature compensation. Unfortunately no strict check on this was made and after about 40 minutes we found that the frequency had shifted completely after a rise of some 5/6 ° [[C-]] without any note having been made of the exact moment of losing control. JMMP has decided that the unit be returned to the

[[NB03-077]]
bench for further tests and a modification giving a manual/automatic switch for setting up. It seems desirable that there should be some method of metering the bias applied to the control valve so that a check can be made that this is not at any time nearing one of the limits.

22-9-50

After discovering that the earthing of the C_{17} changeover relay was producing bad effects from sparking It was decided to set up our switching more permanently and now a switch panel has been set up on the table providing
(a) C_{17} change over
(b) D_9 to E P
(c) Acc clear push button
(d) SCT " " "
(e) O.T. " " "
After eliminating a poor earth connection which gave spurious end pulses each time a tank was cleared, this set up worked OK.

[[NB03-078]]
The E Programme worked every time and so we passed on to G programme. This worked OK until the accumulator became positive when it jammed. Controls effecting the D_9 pulse appeared to be critical ~~and~~ but a position was found where the OT [[passed]] on from the last G. But after one or two tests it was found that instead of stepping on to the next order in fact it stepped on two or three places for apparently no reason.
This was confirmed by trying the next programme

combining E & G orders which always jammed on the G with the Order tank either left with G in it or having jumped to the next compartment but one.
In order to investigate further the single order G O (with the acc negative) was put in store & acted on. This produced a satisfactory state of oscillation which showed that the D_9 pulse was terribly small - about 6-8 volts. It was decided that before further work is done an amplifier will have to be

[[NB03-079]]
put in somewhere to boost up the size of the D_9 (ex G) pulse. Whether this lack of amplitude can have any bearing on

Monday 25 Sept 1950
Lovesay & Co are installing the new voltage control device today so that there is an enforced halt on building of machine. This fits in well with the incorporation of an amplifier in the D_9 line and it has given a breathing space to deal with some other problems that have been neglected. The frequency control unit is ready & waiting for a trial on the machine so that when H T is available we will still not be able to go full steam ahead on the programmes.

[[NB03-080]]

26-9-50
Work on HT control suspended until further notice so work proceeded with E & G Programmes. E programme working quite satisfactorily but G still very obstinate. The chief evidence of the non working of G is that it refuses to step on to the next order when the accumulator becomes positv[[e]] In every case the order tank appears to jump on two or three steps instead of one.
Note is it possibly due to ~~the~~ an extremely long [[time]] constant turning a single pulse into something lasting long enough

to let two or three "1"s into the SCT.
The frequency control unit still remains to be tested.

27-9-50
Frequency control unit installed this morning -- appears to be working OK but later it was decided to introduce screen decoupling to reactor valve in order to reduce FM which was [[apparent]] when input & output pulses of a long tank were compared.

[[NB03-081]]
G order attempted again without success so returned to the E programme. Once again no joy. The E order was then tried by itself and this worked spasmodically sometimes starting from one push of the button and at others requiring a series of End pulses. Some of the trouble was traced to an insensitive (reset) static register which was replaced.
In the process of working the E programme a second fault was located on the Collater - Mixer (dry joint) which was

preventing digits from being added into the accumulator.
Attention was directed to the D_9 & E P for the E order and here it was noticed that there was considerable breakthro of D_9s for a negative accumulator. To overcome this we removed 470 pf from cathode of amplifier and increased the anode load of

the reverser. Now the suppression appears to be complete (tested with Odd D_0 on $40^{1\&2}$) Note one possible ~~fault~~ condition which could have caused confusion is that the flip flop in this circuit is a DC one and

[[NB03-082]]
may need to be reset for correct operation.

28-9-50

Another very frustrating day during which we have gone back about a week & then recovered the ground again.
The first trouble came when at the start the E programme jammed at the U order. Investigation showed some trouble in the PA decoder but after several hours work came to the conclusion that the conditions under which it was being asked to work were completely artificial

and did not necessarily show faults. Retuning to E programme again after several interruptions discovered that it worked OK.
One of the interruptions was again due to the Frequency Control Unit which after having been taken out for a modification refused to work again. I feel that it would be as well to refrain from trying to incorporate a test of the frequency control unit with the already very trying condition of the testing of the coordinator.
Returning again to the G order we decided that the

[[NB03-083]]
end pulse resulting from it was too small. The obvious solution was to use the amplified D_0 which provides the E end pulse & this was done. (This mod calls for a separate cathode follower for feeding the amplified E D_0 to panel.)
This mod produced a very good end pulse but the old trouble of jumping on order after receiving the G end pulse occurred. It was established that it was in fact skipping just one order in this case. This could be due to
(a) The end pulse being

delayed so much as to become a D_2 instead of a D_1 when added to SCT.
(b) in same way 2 pulses both of them D_1's are being passed to the SCT (as for example an End pulse + an R2 end pulse.
It was fairly well established by inspection of a repeating sequence that the pulse was in fact only a D_1 but time (& the HT) did not permit further investigation.
The process used for checking the "1" going to SCT was as follows :-

[[NB03-084]]
(a) A G order placed in position 0 with "1"s disconnected from SCT produced a continuous sequence. The "1"s could then be inspected for position (Positive accumulator)
(b) "1"s reconnected back to SCT and also to Accumulator via AD_4 lead. A single end pulse should produce only 1 digit.
Note in setting up the accumulator to receive "1"s for above test no less than 5 dry joints were found in one half adder.

29-9-50

Investigate whether this jumping of an order is confined G only ~~and is~~ or whether E too gives this jump.

If the latter then there is some grounds for revising our work on D_9 generally.

Tested an E order with marker pulses in various positions in store. Established that the E order does in fact step on to the next position when the accumulator becomes negative.

[[NB03-085]]
Completed proposed tests on G order by first of all adding the end pulses from a single A 1 order into the accumulator via AD_4 This gave location of a correct 1 in the accumulator.
Then a single G order was put in position 0 and carried out. This gave a 1 in the same position showing that under these conditions at least the G end pulse is correct.
In order to check that the G order was in fact still causing a jump the numbers G, I, II, III, etc were put in consecutive

positions in the store with a cleared accumulator.
On carrying out the G order the order tank stopped with the 1 in it showing that it had not jumped.
To confirm this sequences were carried out:-
E E E E E E I II III IIII (neg acc)
showing that even after repetition there was no jumping with the E order similarly
G G G G G ---- I II IIII (Acc +)
showed that G was not jumping
This was repeated for odd (11) and even (10) numbers of G orders in series.

[[NB03-086]]
Performed G ~~sequence~~ programmes satisfactorily. The trouble appeared to be due to a little too much delay in the "1" to SCT before clocking so that a spike appeared in the D_2 position causing the jump. Shorting a couple of sections of the delay line in Coord III did the trick.
Hemy's programmes for right & left shift refused to work but this was the fault of the programme and not the machine.
New & less ambitious programmes proved that

~~right &~~ R & L were both working according to plan but AD_3's did not appear when a D_{35} was shifted right. Frequency control will be installed on monday

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2-10-50

Morning spent installing & testing frequency control. After removing faulty VR65 which was causing quick changes of frequency it seemed to settle down OK although there was some strange movements of alternate lines of the Raster Scope this afternoon

[[NB03-087]]
which might have their origin in the F Control Unit.
This afternoon tests were made on R & L from a composite homemade program it seemed that L was working but R was not. As no shifting programme existed that was self repeating, we devised a new one which shifted a D_{34} to the right 16 times

and then started again. The process was made visible by incorporating a short counting sequence and ~~the~~ a second count of the number of shifts gave a new D_{34}

to be shifted and returned control to the beginning again.
While this programme produced some amusing pictures on the Raster it also suggested that there was a good deal wrong not only with the Shifting sequence but also with the whole setup of adding transferring etc which seems a bit worrying.

[[NB03-088]]

0	T29	
1	A18	First counting sequence time
2	U22	determined by contents of 18
3	E1	
4	T29	clear to Dust bin.
5	A16	Shift contents of 16 1 place
6	R1	right.
7	T16	
8	A18	Second counting sequence
9	A24	counting no of shifts carried
10	U24	out.
11	E0	
12	T29	Clear to Dust bin.
13	A17	Renew contents of 16
14	T16	after x shifts as determined
15	E1	by second count.
16	D34	
17	D74	
18	D32	

This sequence can be used to check ~~right~~ left shift similarly by substituting a D_{19} in positions 16 & 17 and L1 in position 6.

6-9-50

The above programme was used for left shift as proposed and although this gave less trouble from spurious "1"s appearing in the store, the fault of the 1 to be shifted remaining stationary for part of the sequence remained.

[[NB03-089]]
In order to examine this phenomenon more closely the first counting sequence was lengthened considerably and the programme tried again.
Here however more trouble (apparently from the coordinator as end pulses were having no effect) cropped up giving rise to some hours of red herring chasing.
One fact which did arise was that the Transfer unit had to deal with vastly different amplitudes of pulses from the discharge line, those

originating in the Computer (Acc IO) being ~~nearly~~ about 20 volts while those from the store were about 12 volts.
The only apparent solution to this trouble seems to be a reduction of the pulses ex Computer.

Clock pulses to the Store had been previously supplied from the coordinator. These were replaced by the correct Store Clock pulses with resulting in a slight increase in output amplitude.
Frequency Control Unit ~~was~~ was very effective

[[NB03-090]]
on switching on as frequency locked from the word "go".
Apart from one occasion in the afternoon this control has apparently worked very well. On this occasion store contents disappeared ~~with~~ for no apparent reason.

A further reason for lack of amplitude in store pulse has been found. The output CF loads of 1 K had not been changed to 10 K meaning that with at least four Panel 1s connected there was an effective load of only 250Ω. The unit

in use has been changed to 10K with the true load now in the Storage Junction Unit.

The slow left shift program has now been tried again. The first attempt showed that there was faulty coincidence seeking as numbers destined for position 20 were actually finding their way into 22. A minute adjustment of SCT total amplifier corrected this and when the programme was put in again this fault did not recur. There were other faults however. One puzzling effect

[[NB03-091]]
in this programme that has now been solved is that the shifting of the 1 appeared to be delayed for half of the expected time and therefore never completed its expected journey. A much slower repetition (by shifting contents of 18) showed that this corresponded to the time when the second counting sequence became negative ~~and while~~ A reexamination of the program showed that this is correct as although only the D_0 sign digits is effective on conditional transfer, when the number reached D_{35} it gets an extra digit added when it is transferred back into the accumulator

so that although the adding sequence continues the number itself does not become positive immediately but has to wait until another carry clears both D_{35} & D_0 positions During the time that the count is negative the digit is momentarily shifted one place left & then replaced.
Other faults apparant from this sequence were
(a) additional "1"s are being added into the accumulator during the shifting orders.
(b) Occasionally an additional D_{19} (or D_1) is added to the accumulator in addition to the position 18 digit during the first counting sequence

[[NB03-092]]
this persists until the number becomes negative and then clears. This digit has been traced as coming from the multiplicand tank.
Note could this be an explicable programme fault. Check the number of sequences between recurrence of this phenomenon.
======= Later ---------- 4-9-50
Cause of extra "1" mentioned above traced to multiplicand ~~tank~~ register where for some reason the gain control was unnecessarily high. Resetting this eliminated the extra "1"s.
The extra "1" appearing during the shifting sequence appear

to be due to the setting of a pot in the shifting units as there is abnormal breakthro here. Re-setting this seems to have cured the fault but no exhaustive test of this has been made.

[[NB03-093]]

9-10-50

In order to be able to amend a programme already residing in the store, without clearing any orders other than the ones required to be changed :-
(a) Interrupt the coincidence waveform with a switch
(b) Step on SCT to number before that required to be altered.
(c) Restore coincidences waveform
(d) set up revised order.
(e) Send end pulse.

An alternative repeating right shift

0	T18	Clears Acc
1	A15	
2	U17	slowdown count.
3	E1	
4	T18	Clear
5	A13	
6	R1	Shift
7	U17	
8	A16	test no of shifts by adding
9	E0	11111111 etc to shifted digit. When it fails to clear, one is left negative
10	T18	clear
11	A14	replace shifting digit.
12	T13	
13	D34	
14	D34	
15	D26	
16		11111111

[[NB03-094]]

[[stripes]]

[[NO MISTAK Diagram]]

[[NB03-095]]
Queries on I/I.
1) If EP. is sent at end of sequence in order to start the conveying out of Initial orders, a "1" is added to SCT, & 1st order to be commit out is order in Store posn 1.

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