[[NB04-001]]

		64	
1 =	1		128
10 =	1010		256
100 =	1100100		512
1000	1111101000	960	
		32	
		92	

4096 256 16
0000 0000 0000 0000

Conversion numbers
16 - 10 = 6

[[rotated 90 degrees]]
L { -R/L(i - E/R)}
-R(i - E/R
= - i + E
= - E/R(1 - $e^{-R/Lt}$) + E
= - E/R + E/R$e^{-R/Lt}$ + E
= E(1 + 1/R + $e^{-R/Lt}$)

9-10-50

Mechanical means for Dec/Binary Conversion

In order to produce a cheap & simple way in which non technical personnel can enter these order forms with the binary form of information required a machine has been devised consisting of a key operated calculator on which decimal numbers up to 999 can be set (as shown in three windows) while the binary form of the number is automatically set up either in ten other windows or on rubber pads which may be inked to give an impression on the form of the binary number.

[[NB04-002]]
While it seems that this scheme may be useful in the event of requiring say shop order forms to be entered in the binary form, the cost of making such an elementary tool in small quantities may be high.
The idea of mechanical conversion from decimal to binary however should be worthy of greater consideration when it is remembered that if it were possible to make the conversion process part of the inevitable keyboard operation this would eliminate an expensive stage in the high speed input system.
What does such a machine entail?

At present the keyboard operator by depressing each of the keys represent decimal digit in effect causes a partial conversion to the binary form to take place. ~~the~~ The high speed input then takes each of these digits and multiplies them by the power of 10 in the binary form adding together the results.
In order to make the keyboard machine do the conversion, a simple binary counting mechanism must be assumed.This can be in the form of a succession of interconnected cylinders two steps of one cylinder causing one step of the cylinder on its

[[NB04-003]]
left. Now. It is fairly simple to cause the depression of a single digit key to step on the least significant cylinder by one step. Again it seems a simple operation to arrange for 9 keys to step on the least significant [[cylinder]] by increasing steps from 1 to 9. Difficulties arise when dealing with the 10's units however as for 10 two ~~keys~~ cylinders have to be shifted one step and similarly for 100 & 1000, 3 and 6 cylinders. The difficulties which would arise due to having to deal with numbers up to 10^{10} are so many that it becomes obvious that such

a scheme is only practical up to the order of 10^3.
There is however another method of achieving the same object provided that it is possible to subtract as easily as it is to add.
If the depression of the keys were to set up in the machine the [[mixed]] binary decimal equivalents of the number, ie no significance being given to whether the decimal digits are "1", "10", or "100"s then if the necessary conversion numbers are held in the machine, the true binary form can be obtained from the mixed B/d form by the subtraction of

[[NB04-004]]
the conversion numbers.
It is concievable that the ~~binary~~ depression of a key would set up the mixed B/D form while the returning spring would do the subtraction.
E.g.
The number 24 is to be set up
the 20 key is depressed first and this sets up
00100000
as the key is released the conversion
number 1100 is subtracted
to give 00010100
Then the 4 key is depressed to
add 100 to the previous
number giving 00011000

16-10-50.
Before any elaborate form of D/B conversion can be elaborated on the lines mentioned above it is necessary to have some elementary form of mechanical arrangement which ~~wh~~ will perform the function of binary arithmetic.
It would seem that the simplest form would consist of a series of "1" "0" indicators geared to each other in such a way that stepping one indicator on two steps caused the next more significant indicator to step on one step. This action should not be reversable i.e. stepping of an intermediate indicator

[[NB04-005]]
should not affect less significant indicators. Visualising the simplest form of machine then, with the decimal form of the number to be converted given by an operator in a series of impulses for each decimal digit, the fundamental properties of the [[indicaters]] will be:
(a) One impulse to any indicator will change its condition from 0 to 1 or 1 to 0.
(b) Any indicator having its condition changed from 1 to 0 will pass on an impulse to

the next more significant indicator causing that to change from 0 to 1 or 1 to 0.

(c) Impulsing an intermediate indicator will have no effect upon less significant indicators.

With these elementary [[properties]] realised the ability for the machine to deal with more than one impulse at a time must be considered.
An impulse from an operator on the 10 (tens) digit must cause two indicators to be changed corresponding to the form 1010 similarly the hundreds digit requires alteration to condition of three indicators.
In the form of machine visualised above this is not permissible at one time as one binary digit may

[[NB04-006]]
call for a carry from the less significant position thro the ~~second~~ position of the indicator which needs to be changed by the second digit.
eg. if 10 is to be added to 14 then the indicator will originally be in the position

e d c b a
~~1 1 0 1~~
0 1 1 1 0 to add ten

then indicators b & d need to be stepped on. Following properties given above, a change in [[condition]] of b will cause a change in c d and e but if the second digit of the ten is caused to change the condition of d at the same time

no real effect will be achieved and the result will be incorrect.
If however the movement of less significant indicator is delayed until ~~the~~ [[indicator]] c has been change then the two operations will be performed [[correctly]] the indicator d being changed twice.

[[circuit diagram]]

[[NB04-007]]

19-10-50.

After nearly two weeks work on the coordinator / computer building was resumed yesterday. The reason for the break
(a) Long weekend for myself ~~corresponding~~ coinciding with a 3 day holiday for Kaye.
(b) Development work on the frequency control unit in order to rid it of 50c/s frequency modulation.
This presented an opportunity for rack wiring & valve numbering which is still going on.
In the latter part of the break work has been done on the Uniselector Input and it has been established

that with some modification to the relay circuitry orders can be put into the store in the required order. This latter work has been abandoned in a rather unfinished state to allow the uniselector to go to WK for wiring into the starter unit on which they are now working.
Before resuming the original programme of work on the coord/computer we will now go on to testing of output units which have had limited bench tests but which ~~can~~ could be made to print out our computing result.

[[NB04-008]]
Points of interest in the work done recently.
Frequency Control
A [[neon]] stabiliser has been introduced in order to remove as much hum as possible from the +10V +20V and 100V (screen) lines. Time controls have been reduced where possible. Smoothing of the control voltage has been made more effective by [[diagram - 100K resistor + 1 μF capacitor]] rather than [[diagram - 1M resistor + .1 capacitor]]
Dutton is now rewriring this unit.
Starter tests
A [[new latch magnet]] has been installed by [[Mr Lang of Siemens]] who

gave very helpful suggestions on the use of the Uniselector. One point he made was that the wiper contacts should not be used to introduce earth to circuits but that an independent relay should earth the wiper contacts after they had come to rest. This was done by inspecting the relative time of the wiper arms moving around the contacts
It was found that there was considerable bounce in between contacts which before the [[θ]] relay (for earthing) was used caused a number of end pulses to be sent at each step.

[[NB04-009]]
The [[θ]] relay which is a. PO 3000 type introduces sufficient delay to overcome this bounce.

Miss Cox & Miss Plant have been engaged in numbering all the valves in the machine. Various methods have been tried the latest & apparently most successful is to have the number in indian ink underneath a girdle of celotape.

19-10-50

This morning a little investiga[[tion]] was made into the reason why the programme put into the store from the uniselector would not work. It was soon found to be due to a couple of units whose plugs had not been replaced correctly after removal for valve numbering.
Later it was found possible to do the programme direct from the uniselector provided that the switch changing C17± over was made during the homing time of the Uniselector. Having satisfied ourselves that the starter unit ~~w~~ could be made to work ~~two~~ three avenues

[[NB04-010]]
were open for our efforts.
(a) get tape reader working so that programs could be put in to store from tape
(b) get output units working so that information in store could be printed
(c) Continue with computer processes interrupted 2 weeks ago.
The last was ruled out as it was required to get certain tests done on input & output units which required the rest of the machine whereas the computer process programme was a long one which it was undesirable to interrupt.
As Shaw was not quite ready

for tests on output units Kaye & I commenced wiring up relays & tape reader required for putting information in the store (Hemy has provided us with a simplified initial input program which will be sufficient to synthesise orders put in from tape.

[[NB04-011]]

20-10-50.

No progress on Coord Computer due to work on Output Control. Single pulse generator being used to trigger teleprinter clutch. The widening circuit in use for doing this was eventually replaced and eventually Shaw & I were rewarded with the printing of the first few characters ever to be triggered on a teleprinter by L.E.O. Running concurrently with this work the tape reader working set up to read tape but the operation of the [[pecker]] solenoid was so uncertain that it was eventually decided to take it down to realign contacts etc.

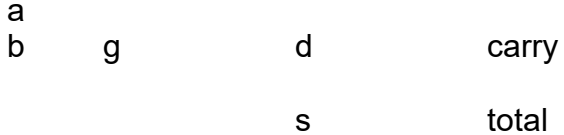
I have continued my investigation of B/D & D/B conversion and while I have not got any definite plans on the latter it seems reasonably ~~sure~~ certain that a mechanical or electromechanical means would not be impossible to design. On the former however I have not even produced a theory that seems likely to produce the necessary.
The method I thought to be the most likely - the adding of conversion numbers - is still the most attractive and still the most baffling. The snag appears to be that in order

[[NB04-012]]
to know how many times to add each conversion number, it is necessary to know the answer.
e.g. to convert binary 10001 (17) into 0001-0110 it is only necessary to add 110
Similarly to convert 11111 into 0001 0101 binary 6 is needed.
In the first case it would seem that splitting the original no into parts and using the most signif to indicate whether to add 110 and where to stop - is possible but the second example shows the flaw in this scheme

23-10-50

A weekend of spasmodic thought has given me grave doubts of ever finding a simple mechanism for making a binary counter.
The difficulties I find are
(a) ~~To avoid~~ ~~Having stepped~~
Having promoted a carry from one digit to the next, to disengage the carry mechanism
(b) Finding a carry mechanism which when operated will not cause a less sig digit to change on the operation of a ~~smal~~ more significant one.

[[NB04-013]]
I have not investigated the possibilities of putting the electronic circuitry of the half adder into mechanical counterparts.



23-10-50

Progress Meeting.
Chase Humphrey re braiding

More work today on Output Units in conjunction with Coordinator. Having managed to stimulate the Teleprinter with a waveform from the Single Pulse Generator, the store was then filled with O_0 orders. Using the SPG to supply end pulses at low speed the teleprinter was then stimulated by the resulting C_{21} waveforms. These were interesting in that they varied

[[NB04-014]]
in length as the waiting time for coincidence changed for each of the O orders.
A new problem has now arisen re the setting & resetting of W_{13}. On 15-9-50 it was reported that trouble had been experienced due to the fact that W_{13} in some cases (particularly when testing) was required to stay up for a long time compared with the time constant of the A C coupling to panel 12. To [[arrange]] this the W_{13} waveform was treated as a negative going one the input value being restored

to 40 volts. In the Output & Input sequences W_{13} is reset by the R_1+R_2 pulse but an end pulse is not received until the teleprinter or tape reader has finished its work so that W_{13} in this case is required to stay down a comparatively long time. Under these circumstances the time constant of the Panel 12 input is still not long enough, being .1x1 = .1 sec. During manual operation of the machine it is desired to inhibit end pulse so that W_{13} will be required to stay up for some seconds

[[NB04-015]]
W_{13} cannot conveniently be reset earlier without mods to circuits but it can be assumed that the waiting times during I&O will be short compared with .5 sec so that an increase of the input condenser to .5 μF would seem to cover the case unless there is a corresponding delay in any of the high speed input & output orders.
It was decided as a temporary measure to use .5 μF input to panel 12 pending enquiries into HS input output circuitry.

In a note on 17-8-50 a report was made of a means of avoiding spikes on coder waveforms due to coincidences of the reset of negative ff & the PA Decoder ff. The remedy of inserting a delay in the common reset merely shifts the spike away from the D_0 position. A better remedy is to delay the reset of the ~~P~~ Action Static Registers but not the PAD f.f. which should eliminate the spike entirely.

[[NB04-016]]
A peculiar fault which was not pursued occurred late yesterday when it was noticed that the W_{13} waveform instead of being normally positive & going negative for the duration of the output sequence appeared to reverse. ~~The details of~~ This phenomenon was not observed in detail but may have been linked with the decay of the W_{13} waveform during the waiting time between end pulses. See previous note.

Supervisors First Meeting

Report on Activities of Past Year
Group Leaders - Campaign
Salary Scale
Office Committees
Electronics in Office

Afternoon Meetings
(1) Companys Accounts
(2) Trocadero
(3) ODC
(4) Export

Business Discussion Meetings
Election
Announcement
Future Meetings (Evening)

[[NB04-017]]
Suitable subjects
Form of Meeting

24-10-50

Rebuilt Freq Control Unit working OK with single modification This was the incorporation of a .1 μF condenser across the 100V line to remove 500 Kc which was being ~~generated~~ injected by the screen of the control valve and causing ripple on widened pulse baseline.
Having incorporated this mod the unit was installed on the machine

(no trace of ŧ F.M. whilst in control condition)

and appeared to work well. The only doubtful quality was that a fairly rapid change of frequency tended to produce ~~of~~ a wobble lasting possibly .2 secs This wobble could also be produced although on a very much smaller scale by shaking the rack vigourously.
~~T~~
An attempt to do a simple program at this stage failed. The orders could be put into the store quite readily but no end pulses were being received from the E & U orders

[[NB04-018]]
The cause of this was whittled down to the fact that (in the case of the E order) S_1+S_2 pulse was falling outside (early) the coder waveform C_{25}
Further investigation postponed pending Supervisor meeting.

Compare “set to ASR” with
S_1+S_2
“ set to ASR “
Coder C_{25}

25-10-50

The article in MTAC No 26 April 1949 on “Conversion of numbers from Decimal to

Binary form in EDVAC" Is, as far as I can see simply a review of the normal processes for DB conversion together with one which I do not yet understand but which does not seem a particularly quick way of doing the conversion.
In view of the space provided for such an article in this journal it seems a pitty that no record (so far as I know has been made of my method of conversion by conversion numbers.

[[NB04-019]]

26-10-50

Yesterday was a day of frustration. The only unit of note which appeared to perform correctly all the time was the newly installed frequency control unit. The first sign of failure came with the first programme tried when after much searching it was found that F_{13} needed two pulses to set it and was therfore not gating S_1+S_2 in the computer to give an endpulse.
A replacement static register was tried before the size of the setting pulses was questioned.
The latter was dependent

upon the setting of P_2 on panel 12. Adjustment of this cured the SR trouble but immediately cause trouble in coincidence seeking circuit. After much trouble a~~n intemedio~~ compromise produced satisfaction on both sides but later programmes showed signs that suggested that once again the amplitude of the set pulse was on the limit.
It would seem logical to provide a separate control for the two outputs from the panel 12

[[NB04-020]]

26-10-50.

Caminer on [[general]] clerical
Requirement

Input Faster - 4 to 8 times
Conversion
More than one source of inf

Theme of Caminer lecture was to illustrate by example how a calculater of the EDSAC type falls short of a GP commercial bookkeeping machine.
He showed that the computer could not be fully employed unless the input & output as used at Cambridge could be speeded up some four to eight times

27-10-50

Yesterdays work on the machine was small in quantity but large in results.
After all the trouble experienced the previous day it seemed reasonable to make some mod even if only temporary to give a larger set pulse for the ASR's while at the same time not disturbing the condition necessary for coincidence.
The main cause of the trouble here is that one control on panel 12 affects the amplitude of both sent to ASR and No to coincidence unit.
The anode load of the Set ASR

[[NB04-021]]

amp was first increased from 3K3 to 4K7. Then turning to Coincidence Unit the anti-coincidence pulse was observed while adjusting the general gain controls of Panel 12 and also the amplifier inserted in the OT output.
A condition was found which was a compromise between a large set pulse and a satisfactory cancellation for coincidence.
With this set up the first programme attempted worked satisfactorily.
Dr Wilkes visited us

just before lunch, and was shown the “alternate adding in two compartment” using E & G orders. After lunch he was shown the continuing right shift program also working very well.
He was quite impressed with the progress we have made and made the comment: “Well you seem to have the greater part of the machine and its functions working.” - This ~~if~~ in front of JRMS was rather unfortunate considering the doldrums we were in the day before.
D.C.’s lecture used up

[[NB04-022]]
the remainder of the afternoon (after a dem of the frequency control unit) but in an effort to restart things again afterwards there appeared to be an intermittent fault on the Clock pulse line which prevented a demonstration of any programme to Mr Pinkerton.

27-10-50
Yesterdays problem cleared. It was due to a faulty SP61 in the frequency control unit - an intermittent dis either on anode or cathode. Nothing at all to do with the control circuit.
Today has been spent mainly clearing two faults. One was hum on the baseline of W8- waveform & the other hum on C17± waveform. The first was an interesting but unexplained case where the connection of two gates to the cathode of a reversing valve was in effect ~~causing~~ presenting a low impedance

[[NB04-023]]
path in parallel with the cathode load of 3K3. This caused amplification of a much higher degree of the volt or two of hum present on the HT line

[[DIAGRAM]]

The cure was to feed the two gates from a separate cathode follower while the [[SP]]61 is used purely as a reverser.

The C17± waveform was produced in the coder :-

[[DIAGRAM]]

This produced hum on each output. By raising the bias on second half of ECC33 to 20 volts, the first half was more definitely cut off and the hum which was apparently being injected on the grid received no amplification. This circuit will need the anode

[[NB04-024]]
loads to be reduced as the voltage output is about 70/90 volts.

30-10-50

Morning at Inquest.

C_{17} amplifier loads reduced to 3K9 & 4K7 instead 5K6 & 6K8. Operating satisfactorily.
During the morning trouble had been experienced with the W_{12} waveform sticking over. This trouble was boiled down to lack of coincidence which in turn pointed to the critical setting of the amplifier feeding the

coincidence seeking circuit.
JMMP had suggested cutting down the amplitude of the gating waveform (D_1 to D_6 D_{19}/D_{24}) to that the pulses would be limited in size to a similar degree and therefore so much more congruous.
This was tried at this stage by splitting the 3K9 terminating resistance of the ~~de~~ line delaying the waveform into 1K5 & 2K2 the tapping gave an output of 10 volts as against 25. This proved to be the answer as the pulses going to the ASR set can now be increased to 30 volts without upsetting coincidence

[[NB04-025]]
A late attempt to do the E/G programme was not successful as the “1” was not added into the accumulator
Another fault which troubled us last Friday was occasional failure of the W1± flip flop. This was cured on Friday by ~~a~~ [[sensitizing]] of the set input of the ff but the trouble recurred today. It is a bit worrying to find a unit as fundamental as this one producing a fault of this type after so many mont[[hs]] of reliable service. There is no indication of serious

changes in valve current that might indicate valve or component failures.

Analysis of Faults.

I think that at this stage enough work has been done on the machine working as a whole to start some analysis of faults. The Cambridge Fault ~~Analysis~~ Record that Hemy abstracted indicated that we probably will continue to have faults for some time yet and it seems likely that a tabulated record

[[NB04-026]]
giving symptoms effects cause & cure would be very useful in the rapid location of cause of future faults. The difficulty probably will be to list the faults under headings that will give quick references and for this reason a card index system might be the best answer. Headings that spring to mind are:-

- W_{12}+W_{13} [[sticking]].
- Coincidence Errors
- Accumulator total incorrect
- Failure to start program

No end pulse
Halting on particular orders

Spurious digits in Store.

Apart from the consideration of the faults to come a complete analysis of past work will be a check on corrections to circuit diagrams which must be examined to be that they have been brought in line with mods made.

[[NB04-027]]

31-10-50

More trouble this morning this time apparently from the coincidence circuit.
The G & E programme worked for a while and then stopped short with nothing left in the OT. All evidence pointed to the ~~ha~~ lack of coincidence in Stage 2.
Examination of Anticoince pulse showed slight breakth which could be almost entirely removed in operation of the amplifier in the counter tank input. This was reset and more normal operation ensued. This suggests that although

part of our trouble on coincidence has been removed by limiting the amplitude of the pulses compared there is still ample scope for improvement in the phasing of the two signals to be compared.
There is still intermittent trouble from two other sources to be solved. One is the $W_1\pm$ waveform which occasionally gets out of step. The other is the counter tank.
The former is possibly caused by interfering with the D_{35} pulse lead (being used for synch)

[[NB04-028]]
Further trouble later with the W_1 waveform caused a closer examination of C.C.U.I. On the Test Rack the unit worked perfectly at any voltage between 200 & 300 ~~but~~ and with a digit pulse at 23 volts. Returning it to the Machine however we found it did not work. Digit Pulse D_{35} was found to be only 18 volts. It is proposed to return CCUI to the bench tomorrow & either make it more sensitive or else convert it to a D.C. F.F.

2-11-50

Back on the Test Rack CCUI ff refused to go on any pulses less than 18/20 volts so decision was taken to modify to DC flip flop

[[DIAGRAM]]

[[NB04-029]]

Input / Output

INPUT 36
(1) Speed.
(2) Binary
(3) More than one source at once.
Magnetic Tape.

120 yds characters
1.12 cm per characters
8 cm sec normal
48 " " high speed
= 42 characters/sec

Why store tape in box.

Output
High Speed recorder
160cm per sec

[[DIAGRAM]]

[[NB04-030]]

[[DIAGRAM]]

CCUI

[[DIAGRAM]]

[[NB04-031]]
DC [[of flops]]
If trigger valve was made an amplifier instead of [[l l^5]] the FF could be triggered on the grid with a negative [[?]]pulse ~~of~~ the amplitude of which would not be so much determined by the input pulse which in present [[wires]] is often very small.

7-11-50

Coordinator
(a) Breakhthro of SCT "1" in position after D6. →
(B) Phasing of D_1D_6 waveform.

Investigation of cause of W_{12} sticking in set condition
(a) Store full of Add "1"
(b) Count No of S_1+S_2 & compare with no in SCT after W_{12} fails
(c) Count no of R_1+R_2 & compare as before.
Result of (b) showed that coincidence unit was being stimmulater
Result of (c) suggested that failure of W_{12} occurred thro lack of R_1+R_2

[[NB04-032]]
Removal of "EP from Computer" from Coord enables this process to be followed one step at a time

Breakthro of digit pulse after D_6 as mentioned in (a) due to common cathode load of 3K3 in CF feeding the D_1D_6 waveform to gates of coincidence seeking circuits this has now been eliminated by reducing to 1K5

A cross talk effect noted by Shaw on the Test Rack between two long tanks one

being used for the Machine store was found to be due to feeding Test rack ~~output~~ input from same end of Battery as the Store input.

7-11-50

Gas Discharge Tubes

Neon 92[[%]]
Argon → impurity
Hydrogen 7 → for reducing [[deconisat??]] time

[[NB04-033]]
Simple element

[[diagram - Anode Cathode]]

[[DIAGRAM]]

Flip Flop

[[NB04-034]]
Pattern Register

[[DIAGRAM]]

Pattern may be injected from one end one pulse at a time or in parallel
Max f of multi calls 10/50 Kc

Output of pattern generator obtained by pulsing input tube successively.

8-11-50

Since the break in our building programme occasioned by the introduction of the frequency control unit about a month ago very little progress has been made. At that time the sequence being investigated was Right & Left shifting. Since that time apart from some small progress on the input output units we have moved back rather than forwards. I feel that the reason for this is largely ~~a~~ due to our method of approach ~~me which lacks~~
What are the problems which

[[NB04-035]]
have to be faced. They are
(1) More and more circuitry is being brought into play in order to do ~~the~~ more ambitious programme.
(2) With the extra circuitry come new faults & imperfection which may be quite subtle ~~and~~ in their expression.
(4) With more complicated programmes circuits which have not shown any faults previously show up imperfection previously hidden
(5) With more circuitry the prospects of component failure due to ageing and

fundamental faults, grow.
A consideration of these points shows that the present method of dealing with faults as they present themselves is bound to lead to confusion. At present when a programme fails to work an attempt is made to find the cause and correct it so that the programme can be proceeded with. This is completely wrong. Before any fault is written off as having been corrected and analysis of its effects must be made and if the circuit in which it occurs has been in use

[[NB04-036]]
before it must be established whether the fault has always been there or whether it has just developed. If the former then why it has not been apparent before and what the implications are of its correction. If the latter then is it a ~~fund~~ fundamental fault itself or has it been caused thro working conditions.
In this way the experiences of fault finding will be much more useful and if a detailed analysis of faults is kept - and it should be kept

From day to day - then subsequent faults will be easier to analyse.

Later

It was agreed that a new approach should be made to work on the computer on the line mentioned above.
First - instead of trying to keep a record of events in the diary in my own time, a fault sheet is to be made out for each fault as it occurs with a detailed description of its investigation.
From these fault sheets a summary will be prepared which

[[NB04-037]]
should provide a quick reference to faults.
In the investigation of faults the following points need to be borne in mind.
1.(a) Is the fault new or (b) has it been present before undetected
2. If (a) then is it fundamental or does it arise from a second fault possibly a design fault.
3. If (b) Why was it not detected before and what are the implications of its cure.

It was also agreed that more time should be given to the consideration of how the

problems should be tackled and that reference back of faults and proposed programmes should be made weekly to J.M.M.P.

9-11-50

Work proceeded well under new scheme with 6 Fault sheets made out already and only one complete.
The biggest improvement is in the state of mind ~~wh~~ with which one can approach new problems. One fault run to earth today was the insensitivity of the reset of PAD ff. In view

[[NB04-038]]
of the fact that there may be many places in the machine where pulses are barely sufficient to keep things going it would be as well sometime to ~~inhibit~~ institute a general test throughout the machine with a standard ~~20%~~ x db attenuator ensuring

that various functions are carried out with pulses x dbs less than they normally use. One thing that this will not cover is any test on increases in breakthro

21-11-50

For many weeks now a certain pattern of W_{12} waveforms has been accepted as an indication that the coordinator is correctly following a repeated ~~add~~ any sequence with the store full of the same order eg A_1
This pattern is one of 32 waveforms with starting with a fairly wide one and gradually diminishing until at the 20th a change occurs and it is followed by 12 apparently of equal size. It has never been explained why there should be this change half way thro the pattern.

[[NB04-039]]
160 144 128 112 96 80 64 32 16 0
176 224 256 320
16 16 272 336
192 240 288
208 304
As the order in all positions is the same it is reasonable to suppose that the time taken to find coincidence will vary considerably but should start at one instant at a length of say 18m/c and then diminish to two m/c.
Assuming that the order is A_0 and that the first end pulse triggering the sequence is $0D_0$. Then coincidence unit [[in step]] at $1D_{18}$
R_2 triggers Add in computer to let an odd D_0 thro for end pulse. R_2 itself may be an odd D_0 but there is no delay to ensure that a full pulse is gated.

[[binary / register calculation]]

[[NB04-040]]
[[double page spread]]

EP $0D_0$ ~~$18D_0$~~ $34D_0$ $66D_0$ $98D_0$ 130^0
162^0 194^0 226 258 290
W_{12} [$0D_0$ $17D_0$] [$34D_0$ $^{50}D_0$] $66D_0$ $82D_0$ $98D_0$ 115/0 130^0 147^0
162^0 180^0 194 212 226 245 258 277 290 310
S_1+[S_9] $1D_{18}$ $18D_{18}$ [$35D_{18}$ $^{51}D_{18}$ $67D_{18}$ $83D_{18}$ $9D_{18}$ 116/18 130^{18} 148^{18}
163^{18} 181^{18} 195½ 213½ 227½ 246½ 259½ 278½ 291½ 311½
$16D_0$ $32D_0$ $48D_{18}$ $64D_0$ $81D_0$ $96D_0$ 113/8 128/0 145^0 160^0
178^{18} 192^0 211 224 243½ 256 276 288 308½ 320
Coince /D_{18} /D_{18} /$49D_0$ $64D_{18}$ D_{18} D_{18} D_{20} 5K 18 18
179^0 18 ½ ½ 244 309
R_1R_2 $17D_0$ $33D_0$ $50D_0$ $65D_0$ $82D_0$ $97D_0$ 115/0 129 0 147^0 161^0
180^0 193^0 212 225 245 257 277 289 310 321
W_{13} [$17D_0$ $33D_0$] [$50D_0$ $65D_0$] [$82D_0$ $97D_0$] 1

SCT 0 s 0 1 0 2 0 3 0 4 0 5
0 6 0 7 0 8 0 9

17 16 16 17 17 18 18 19

19 20 20
W_{12} [0 17] | 34 50 | 66 82 | 98 115 | 130 147 | 162 180 | 194 212 | 226 245 | 258 277 | 299 310 | 322 342 | 354
17 16 16 15 15 14 |
| | | | |
Coince | 14 |
13 | 13 1|2 | 12
Coince
| 321
Stage 1 Coin = (2n+1)16 + n/2
| 341
Stage 2 Coin = (2n+2)16 = 32(n+1)
342

23
176 32 32
2½ 6 46
178½ 192 9
73

[[NB04-041]]

~~EP~~
~~W_{12}~~
~~S_1~~
~~Coin~~
~~R_1R_2~~
~~W_{13}~~
~~SST~~

JMMP on the Converter
two kinds of inf Nos & Control

from tape
m/c -->---------- __Translator----------Control---------->No [[Bd]]
| (Decoder) (Coder)---------->Block [[End]]
| |
| Arithmeter---------->Information to Array
| | ---------->Marking Pulse
| |
10Kc/s Timing Circuits

Space inspection time
Mark 1 2 3 4 5 6 7
Start Stop

Time Scale produces inspection pulses

Normal TP speed 140 ms per [[illegible channel?]]
High Speed for convertor 21 ms "
Time scale starts at beginning of start
No 1 ---------- 3 m/s
4½
7½
10½
13½
16½

Start & [[intallyer]]	Stop	Next character
transfer to arith	arithmeter	also feeding to calc of first No

[[NB04-042]]
[[double page spread]]

Time Scale Circuit

Triggered by start impulse

(a) Divide by 3.

[[Circuit diagram]]

+10Kc/s 300μS ----------> every .3 mS

10counter 3mS ----------> every 3mS

-10Kc

7counter ----------> every 21 restors to starting condition

[[NB04-043]]

Decoders

[[DIAGRAM]]

Arithmetic Unit

[[DIAGRAM]]
12 Wire Coder
Digit Register & tubes
Add
Mier x10 x2 x12
Register

Multiplier

Shift ---- Add

[[NB04-044]]

Additional test equipment of the go-nogo type.

(a) Phase misalignment of .1μS

(b) Zero restoration faults checked by 18 digits followed by 18 spaces. (this could be provided by number selector.)
(c) Means of varying voltage on one panel at a time by ±10v (not very easy)
Could be provided on an unused terminals on the 12 way [[block]] ie +260v and -210 volts [[stabily]] and with sufficient capacity to supply heaviest single current drain

21-[[11]]-50
In doldrums again in spite of new fault sheet system that seems to work quite well. Today, having got the coord loop working quite satisfactorily tried an add sequence. This would not work apparently due to lack of end pulse from computer. Same thing applied to E order. Work on computer in an attempt to find fault was obscured by the fact that W1± decided to stop periodically.
The lack of an end pulse causes the Coder waveforms set up as a result of the order to remain "up". As all these

[[NB04-045]]
are AC coupled to the computer the effect of the next EP sent from the SPG in an attempt to investigate the trouble is to reset the coder waveform after [[all]] the coupling capacitors have been fully charged
---
Wilkes wishes that he had installed some such go nogo tests earlier, but did not suggest that they were doing so now.
Photoelectric - [[no snags]]
Cost of teleprinter mods about ⅛ of capital cost.

½ Teleprinter Mods
Bits for Tape Reader.
Who [[supplies]] contacts?

Maths Lab want to get on with Tape reader. What about bits & pieces.
Who is supplying

EDSAC Just out of 2 weeks of Doldrums. Renwick [[installing ?]] new set of tests.
Magnetic Drum 4" with flywheel 8 leads each 8 tracks = 64 majorcycles 3 secs for half [[divide]] tracking. Inhibition while tracking.
Wilkes book on Programming

[[NB04-046]]

23-11-50

ACE ----------

DSIR about to publish work.

32 B.D.

32 words 3 8 tanks
1 Mc/s 1024μS.
256 words. (½ [[Edsac]])
10 short tanks ("Temp Storage")
2 for timing 8 storage

Source	Test	Time	Time	No of Tank
5	5	6	6	3
			Wait	

36
16
216
36
576

[[DIAGRAM]]

? 3x9 digit on card

100 cards per m
1200 numbers

Output either B or D
Manual input 32 switches
32 lights for output

[[NB04-047]]
[[Pluses]] ---------- ?

43 panels.
18 circulation
14 Basic Pulse & input output
2 Control
1 Add Subtract
3 Mutliply
1 Hollerith in out
1 logical
[[Thermostaticall]] control coffin but short tanks not controlled

Test program

Table of squares to 100 printed Hollerith [[clards]]

Prep for magnetic drum

[[Crile]] ¾" 2'7

[[NB04-048]]
GARWICK, JAN V.

Electronic Component
Weedon Rd Industrial Estate
Northants

Mr Cator
Jones type plugs & sockets
with sealed in (neoprene &) [[leaves]]
6 + 12 way

Possible Mod to CCUI

[[DIAGRAM]]

[[NB04-049]]
Control Circuits

Character	Purpose	Condition Reset by
Start. S.	To start Conversion	End +
End +	To indicate end of tape	Start S.
Long No L	To indicate 35 digit register required	Car Return
Space	To indicate end of 1st short No	Any character
Car Ret	End of 1 long or 2 short Nos	Any characters
Line Feed	One line feed has no special significant	Any character except LF
	Two line feed - end of block	
	Third line feed confirms Block end	Any other character
Colon	1st colon selects x2 for next character only	Any char
	2nd colon select x12 for next character	Any char
Minus	Puts - into 17th or 35th position (follows no)	Requires no reset
Designation star	Causes subs digit to be marked into position 31/34 or 13/16	Car R or Space

Other characters
Insert Quotes (new matters)
Remove Brackets (deleted)
Print Out
Integer Point

Comma

[[DIAGRAM]]
T pulses Information Pulse
100μS Marking Pulse
[[r]] pulse
counter 36

NE No end
16 Block End Pulse
Test Just Ready Tube empty±
before BE
but not Unready Tube Full±
afterwards

[[NB04-050]]

8-12-50

Programme for Resumption of work on Coordinator after shutting down for consolidation of modifications and valve numbering
(a) Coordinator Rack.
1. Counter Tank.
2. Sequence control tank
3.
All OK Testing continuing with R & L shift

11-12-50

Testing of R & L orders.
(a) No in acc which can be easily recognised.
(b) Set up Rn on No simulator
(c) Input to Store position 0 (D_9)
(d) Execute order (D_9)
(e) Set up Ln on No simulator
(f) Input to Store
(g) Execute
(h) Set up Rn+1
(i) Input
(j) Execute
(k) Set up Ln+1
(l) Input
(k) Execute
etc etc.

[[NB04-051]]

12-12-50

Mods required.
(1) Amp & Delay in PAD
(2) Reverse W_{16} in LC27
(3) TCTSU W_{16}- to two gates
(4) TCTSU Unamplified Dh to mixer
(5) Coord II W_{12} & W_{13} mods as arranged

12-12-50

Reconversion [[TBD]]
(a) Notation LSD - lbs etc
(b) No of digits
Presentation decided by programmer
for every number to be printed there is a presentation number which decides exactly how the number is to be presented.
Digits of presentation No give
Print or C/1^5
Car Ret
Line Feed
No of Digits
No of Spaces in front of No
Presentation No first.
? Why long nos
? Indication of How many in multiple presentation No

[[NB04-052]]

[[DIAGRAM]]

13-12-50

Programme
(1) Continue investigation of spikes on Coder waveforms as planned.
(2.) Someone to make up new tank but before this is done precise measurements of pulses going thro tank to be replaced. Mier Tank is obvious one to be used.
(3) When Hemy has produced shifting programme test left & right shifts in accumulator.
(4) Proceed with remainder of tests of orders ex coordinator including go-nogo tests
(5) Test new tank when ready.

[[NB04-053]]
~~(5)~~
Jobs required to be done.
(a) Article on Graphical Representation
(b) Two indicator units (pair) for ff
(c) Index and Pulse & Waveform index for notebook.
(d) Wheeler to get rings and nylon for RC crocks.
(e) Alteration of Diagrams to keep ~~place~~ pace with mods carried out.

Gibbs	-	Tank tests & possibly neon indicator.
Wheeler	-	crock clips
		flip flops
		chassis for Indicator
Miss Cox	-	Article
& Miss P.	-	Index etc.
	-	Diagram Mods
	-	Valve Numbers.

Dutton Unit Testing
Supervise Wheeler
Neon Indicator
Shaw Supervise Unit testing
Assist Coord Tests.

[[NB04-054]]
Method of testing Coder waveforms

Set up order in position 0 of store
Remove "1" from SCT
Start sequence.
Examine all waveforms from PAD to Coder Outputs
Required - ruled sheet on which to record comments.

PAD.
S_2'
Reset
W_{16}±
W_{17}±
Routed W_0
" $_0$
1
1
2
2
3

During yesterday it was established that the criticism levelled against the Micand SU (ie that it includes an amplifier which produces unwanted delay) is true also of TCTSU.
It was found that shifts of up to 10 places were possible but that after this time the Dy went out of circulation. Attempts to get a circulation ~~with~~ artificially (thro TCTSU) failed although the tank itself behaved normally.

[[NB04-055]]

14-12-50

Today Orders X Y and H were satisfactorily cleared. A really troublesome fault on Shifting which permitted a Right Shift of ~~49~~ 15 places indefinitely ~~and a few~~ but would not permit a left shift of more than 10 places was at last located to the lack of DC restoration on the C5 input of TCTSU
The clue which led to the solving of this problem was that L_{15} persisted almost every time for 49 orders before failing. This was equivalent to a time of 1-2 secs which in turn suggested a RC of .1μF & 1MΩ

R
L
Required - program that will put number into accumulator & shift L_1 R_1 ~~R~~ L_2 R_2 L_3 R_3 etc with counts in between shifts to enable faults to be seen

(a) Assume number can be introduced into accumulator artificially.

T_a	Transfer number to Store
A_b	double No in b
A_b	
A_c	make up Left order
T_d	
^{d}	left shift
T^f	
A	
U	
E	
T^g	
A_b	
A_b	
A_e	
	Right order
AU^f	

[[NB04-056]]

T_a	Number to Store		
A_b			
A_b	Double up Shift digit		
U_b			
A_c	Make R order		
T_d	Transfer to d		
A_a			
^{d}	Shift		
T_{fa}	Transfer WPB		
A			
U	Count		
E			
T	Clear		
A_g			A_d
A_b	Make L order	G	
T	Transfer to h		
A_a			
	Shift		
T_a			
A			
U			
E			
T	Clear		
E_1			

1101

0	T_a	31	Number to Store
1	A_b	15	
2	A_b	15	Double shift digit

3	U_b	15		
4	A_c	16	Make R order	
5	T_d	~~30~~ 7	Transfer to d	
6	A_a	31	Shift	
7				
8	A	18		
9	U	30	Count	
10	E	8		
11	T	29	Clear	
12	A_e	17		
13	A_b	15	Make L order	
14	G	5		
15	D_{19}		0	Number
16	R		1	Shift digit
17	L		2	A_1
18	D_{28}		3	A_1
			4	U_1
			5	A

11111

[[NB04-057]]

Programme

(1.) Check new minorcycle Tank
(2) Remaining Orders
- (a) Collate
- (b) multiply
- (c) left Right Program

(3) Mods
- (a) Coord
- (b) ~~Transfer~~
- (c) PAD
- (d) Decoders
- (e) Shifting Units
- (f) Other Computer Mods

(4) Valve Numbering.
(5) Proceed with
- (a) Subtraction
- (b) Addition of Digits
- (c) Long / Short Numbers.

28-12-50

Position in testing of machine now quite good.
A fault on the second Half Adder of the accumulator had been obscuring the Position on Right & Left shift but this has now been traced
Sequences checked now include everything with short positive number with the exception of subtraction

There are a number of modifications outstanding some of which will be put in this weekend when a new Satturday Rota starts.
This morning a final check on shifting should clear this sequence and let us move on to subtraction and negative numbers.

[[NB04-058]]
Try a new Shifting programme :-

	0	Number	
	1	Add $_0$	
00100 R	2	R_2	
11001 L	3	L_2	
	4	R_3	
	5	L_3	
	6	R_4	Observe number
	7	L_4	in accumulator
	:		
	:		1110111011100
	22	R_{12}	11101110111
	23	L_{12}	10010101010011
	24	R_{15}	
	25	L_{13}	

If Inhibit EP is held down then this can be done at varying speeds by the SPG.

This should be considered as a supplementary test to the normal which gives a more stringent test for limited size numbers.

	0	Number	1110111
	1	Add 0	
	2	L_x	9
	3	U_0	
	4	R_x	9
	5	T_0	
	6	E_1	

This program can be permitted to run at normal speed

[[NB04-059]]

Mods

Coordinator
Prim Action Decoder
Shifting :- TCT SU
CCU
Collater
Complementer

29-12-50

Quite a lot of progress made yesterday. With shifting confirmed in the morning I went on to subtraction which worked first time. ~~Add~~ Going on to negative numbers - Add was OK but subtraction of negative numbers gave rise to batches of 1s in the less significant half of the acc. Inspection showed that the flip flop in the Complementer

was not being reset every time by ED_0
If amplified ED_0 is used however this fault is cleared.
The programme from now on is as follows

[[NB04-060]]
Today (1) Right shift of negative numbers
(2) Multiplication with neg mier
(3) V with neg micand
(4) V with neg mier [[next]]
Prepare for mods to be carried out tomorrow.
Prepare for discussion on new machine.
Mr Neil Salmon was shown work in progress on the machine yesterday we had single shot addition and subtraction working Adding a number 4 times and then subtracting it 4 times.
This was done repeatedly

(and correctly)
Mr Thompson gave examples of the use of long short discrim position digits in orders not requiring transfers to & from accumulator

[[NB04-061]]

2-1-50

Outlet Annexe JMMP

Between calculator & Reconvertor.
Purpose
(a) Reception of up to 16 long numbers in a group from Calculator when empty
Indicate & prevent when full
(b) Unload one number at a time digit by digit to the reconvertor
(c) Has to recognise signals from ~~indic~~ reconvertor indicating :-
1 end of number
2 end of group
3 Unready signal

Required - checking device

For Decoder system

[[DIAGRAM]]

Step on SCT one place at a time.
Remain in
(1) Inhibit EP
(2) SCT / OT switch.
(3) Step on SCT ~~or OT~~
by SPG. (D_0 to SCT D_{30} to OT
(4) Observe neon indicators for T N and Coder outputs

[[NB04-062]]

[[DIAGRAM]]

From Coders
Via DC Amp.

32 for Coders
2 for F_1 F_2
64 for T N.

DI
(1) Valve Alright
(2) Neon Alright
(3) Counter Counting
(4) W_1
(5) Reset all FF
(6) [[Coder]] check
(7) Test Programme

Mods to be done

(1) Micand SU.
(2) Transfer ~~Tank~~ Unit.
(3) Amplify DNV
(4) Delay & Amp Reset to ASR
(5) Mods to Decoder
(6) Mod to prevent partial multiplication during shifting.
(7) CCU II
(8) FF in CCU VIII (LC 32) for AD3
~~(9) ? Mods to teleprinter.~~

[[NB04-063]]

Programme Preparatory

(1) Press for shortened tanks
(2) WK for starter
(3) Tape Reader
(4) Op Counts of Units
(5) P.S.Units
(6.) Function Box
(7)

Immediate Work

(1) Long Nos
~~(2) Output Units & Teleprinter~~
(2) Tank Decoding
(3) Output Units & teleprinter
(4) Starter & Tape Reader
(5) Attenuator Checks

(6) Fill new battery
(7)

[[NB04-064]]

Suggestions for
Progress matching 4+51

(1) Shaw & I complete present programme of working sequences with long numbers and connecting up other tanks using decoders.
(2) Gibbs should work on preparing diagrams & panels etc needed for Input & Output.
(3) Gibbs assisted by Wheeler should prepare for new long tanks - cables etc. ? are these not ready ?
(4) Dutton should complete bench tests on units required for input & output and also attend to any units requiring maintenance as machine tests are carried out.
(5) Modification to units and

completion of valve numbering should be done as and when machine is out of action.
(6.) WK should be pressed for delivery of starter units and any other necessary unit required for input/output.
(7.) As soon as Coord Computer Tests and Mods are complete Gibbs & I start work on Input or Output according to availability of components.
(8) Programmes should be prepared by Hemy & Co giving
~~(a) for input a tape which is conjunction with Starter Unit will put well defined pattern into~~

[[NB04-065]]
store.
(b) Programme which can be ~~up~~ put into store by hand and which will represent typical output programme.
(c) Programme on tape which with Starter Units will put in information for the machine to carry out and provide necessary orders for it to be printed.
9. Some thought should be given to system of monitoring all store positions.
10 Hand over machine to Kaye & Shaw
11) Fill second battery

Possible Dates

12-1-51 Coord Computer tests complete with ~~15~~ 15x16 storage ~~tank~~ positions available. Reservations on reliability of computer pending marginal tests.
19-1-51 Preliminary tests on Output Units & teleprinter complete with machine able to print via temporary wiring
26-1-51 Machine able to take information from tape into store ~~but not~~ and able to work on it ~~without~~ with programme set up by hand.
2-2-51 Starter working
Machine able to work from Tape and [[illegible]]

[[NB04-066]]

Secondary Jobs
(~~when~~ pending completion of EDSAC replica.)

(1) Preparation for Filling Second Battery
(2) Prep for monitoring store contents
(3) Major cycle Pulse Generator.
(4) Mods to Neon indicators
(5) Second Flip flop indicator pair

Jobs after EDSAC Replica

ie during testing of HS I/O
(1) Fill remaining Batteries
(2) Design of test apparatus
(3) Manual
(4) Control Desk
(5)

[[NB04-067]]

What should a Daily Test Programme Do.

(1) Put easily recognised pattern into store
(2) Put series of short repeatable programmes into store and carry them out one by one with alarm if any sequence fails
These programmes should all be progressed and result in an easily recognisable state

4-1-51

At a meeting with TRT JP EK & RS today the first real ideas on the completion of he machine in the EDSAC form were aired. It is generally agreed that Shaw & I should continue work on the coord computer tests until long numbers have been dealt with and the tank No decoding system tried out to deal with [[??]] [[panel]] 1. When this and any outstanding computer mods are completed Gibbs should start with me on
(a) Output
(b) Input
(c) Starter
after which

[[NB04-068]]
the machine should be usable for small programmes.
It is proposed at this stage to make the machine operational for a short period each week in order that the organisation of clerical work fed to the machine can be tried out.
It is also proposed to stage a demonstration of the machine at this stage in order to ~~create~~ produce the required enthusiasm for [[illegible o---t--n]] of further progress.
During the past few weeks the faults have been occurring fast & furiously but we

have kept our heads above water and at this moment all sequences have been tested for short numbers and we are about to proceed to work on long numbers.
One fault in hand at the moment is the occasional mistake of the coincidence unit. It occasionally find position 4 instead of 5 etc appearing to ignore the least sig digit.

5-1-51

This is most probably due to too much delay in waveform gating counter & SCT in LC 45

[[NB04-069]]

5-1-51

The problem of how to inhibit partial multiplication in shifting operations has to be considered.
It is required that ~~a multiplicand~~ the mier register holds its number until it is cleared by a new hold order so that it seems that the simplest procedure is to make the R or L order clear the Micand tank.
This seems to be most easily done by adding C_5 or C_6 as an mixed input to LC 39
This will mean that the micand Tank will be cleared by A S C V H R L

This raises the point :- why not clear multiplicand register after every sequence irrespective ie let S_1+S_2 set W_{11} every time.

[[NB04-070]]

8-1-50

Tests on long numbers now proceeding. Success with Add Subtract ~~and~~ multiply & Transfer but for some reason Copy does not work. The process of checking long number arithmetic is a bit tedious.
I badly need some technique for recognising results easily.
Mr TRT has produced a programme which the m/c will not do at full speed although it can be done at quite high repetition speeds on the SPG
This was demonstrated to Mr Sim who I think was not

terribly impressed.
In order to test the U sequence

0	A_{4L}		
1	U_{6L}		
2	E_0		
3	-		this digit to be shifted
4	D_{19}		to give varying results
5	-		
6		Count	
7			
8			
9			

[[NB04-071]]
Add & Transfer have been tested for varying numbers but not negative ones.
Left shifting 8 at a time has been used successfully

A_x	0	A_{11}	L
L_4	1	L_{11}	
S_x	2	T_{11}	L
S_x	3	H	
S_x	4	V	

S_x	5	S
S_x	6	A
R_4	7	A
A_x	8	U
A_x	9	E
A_x		
A_x		

~~0 N_0~~
~~1 T_{31}~~
~~2 A~~
~~3 L_4~~
~~4 T~~
~~5 H~~
~~6 V~~
~~7 S~~
~~8 A~~
~~9 A~~
~~10 E~~
~~11 E~~
~~12~~
~~13~~

~~0 N_0~~
~~1~~
~~2 T_{31}~~
~~3 H_0 L~~
~~4 L_4~~
~~5 T_{28}~~
~~6 H~~
~~7 V~~
~~8 L~~
~~9 A~~
~~10 A~~
~~11 E~~
~~12~~

Holders for neons

[[NB04-072]]

0	T_{20}	
1	S_{12L}	Puts -1 (long No)
2	T_{16L}	in 16 collaters with
3	H_{14L}	1111 putting result
4	C_{16L}	in 18.
5	T_{18L}	
6	A_{14L}	
7	L_4	At every loop collate
8	U_{14L}	number is shifted
9	E_0	
10		
11	D_{19}	
12		
13	1111	
14		
15		
16		
17	Results	
18		
19		
20		

Right shifting of number & transferring

	0	A	10	
A	1	T	LL	
R	2	T	31	
	3	A	12L	
	4	R	4	
	5	T	12L	
	6	A	11	
	7	U	30	
	8	E	6	
	10	G	2	1101011
	11			
	12			
	13			
	14			
	14			
	15			

[[NB04-073]]

I 9-1-51

Reconvertor.

1. Receive Inf from Outlet Annex
~~2~~ Numbers - Instruction Coposition Multiple
2. Control flow of information
3. Reconvert Binary Decimal.
4. Interpret Composition instruction
5 Pass on reconstructed Nos to Compositor.

Information

Marker Pulses
every 1.12 mS
Up to 36 - 36 for compositions
Up to 35 for a number.

Digit

500 to bogus.

Composition Instructor

Control of flow

1. Rv counts marking pulses up to 36
2. Emit n.e.p. After 36th
3. Count nep & issue b.e.p. on 16th (or earlier if indicated by comp instructions
4. Emit Unreadiness condition to stop flow from outlet

[[NB04-074]]

9-1-51

Fairly successful day with long numbers satisfactorily tested
Before going on to Decoding I am attacking TRT's programme again & I feel that there are good hopes of success.
There are two faults I think shown up in the programme one is the remainder left in Acc after completing the sequence, the other is the fact that at machine speed, the sequence always stops on order 26 (a single 1) with a positive accumulator. As the previous order is E_0 this suggests that E is not

producing a D_9.
I have produced a simple programme simulating the second part of ~~the~~ TRT's programme and this too falls down on subtraction of all things.
While this may give a lead to some trouble in the computer I am not concerned to any extent as I feel it may merely disclose a time constant in a circuit which needs a small change

[[NB04-075]]

Programme to simulate
last part of TRTs programme

0	A_5	1111111111111111	"1" to extend into sign digit
1	S_6	11111111	
2	S_7	11111111	
3	E_0		
4			
5	16 1·s		
6	8 1·s		
7	81·s		

If this works OK
Introduce some shifts.

0	A_9	
1	R_7	In this case
2	R_8	"1" should not originally
3	L_8	extend into sign digit
4	L_8	inorder to avoid complication
5	S_{10}	of AD_1
6	S_{11}	

If first programme does <u>not</u> work.

(a) Investigate subtrahend input to half adder.
(b) Try effect of adding 1 instead of subtracting

[[NB04-076]]

Programme for work on
<u>Decoding.</u>

~~(a) Introduce Decoders onto input of store Rack 0 P~~
(a) Test panel 1s and storage ~~units~~ tanks associated with Rack 0 for circulation of 1s

(b) Introduce Decoding into input to Store & check by inserting orders into all Rack 0 store units.
(c) Introduce Output Decoding and test by inserting

~~A~~

0	A_0	0	A_2
1	U	1	A_5
2	E	2	U_5
		3	E_1
		4	1
		5	1
		6	1
		7	1
			:

10-1-51

Fault causing TRTs programme to fail has been found. It is due to insufficient amplitude of number pulses going into Complementer. A temporary solution has been found in increasing amplification in the complementer but this may not be sufficient to ~~wu~~ stand up to attenuator tests which have not yet been done on the Computer.

[[NB04-077]]

From		To
~~CCU III$_{27}$ (Black)~~	~~TCTSU~~	~~19^{12}~~
~~Acc Clear~~	~~Push Button~~	
~~Amp ED 27^6~~		~~29^4~~
~~Reset 29^{12} to Crock~~		
~~Amp ED$_0$ 29^4~~		~~17^6 28^5~~
~~TCTSU 19^6 → Amp DVN → TCTSU~~	~~31^2~~	
~~LC20 2 pin Plug~~	~~C$_{17}$ switch~~	
~~11^8 D9~~	~~Switch~~	
~~10^2 EP~~	~~“~~	
~~Trigger SPG~~	~~D$_0$~~	
~~Trigger SPG~~	~~D$_{33}$~~	
~~46^4~~		
50^{10}	CPt Store	

Mods

CCU V	LC 29
CCU X	LC 40

V_{17} A had been restored to about +40 instead of +35. I believe this was a despairing effort to produce EP5 without a D_q and which was achieved by a change to anode load of V_{15}

Coincidence II	46.
Transfer Unit	36
CCU II	26
~~CCU X~~	~~40~~

~~CCU V 29~~
Micand SU 24
Complementer 17
Acc I.O. 37

[[NB04-078]]

SCT.		Store Pos	
~~0~~	2	0	~~0~~
~~1~~	4	3	~~1~~
~~2~~	5	5	~~2~~
~~4~~	6	6	~~3~~
	7	7	
	8	8	
	10	9	
	14	13	
	16	15	
	18	17	
	20	19	
	22		21
	24	23	
	28	25	
	30	29	
	32	31	

10-1-51

Reconverter

Marker Pulse (36)

Marker Pulse Counter

Information Pulse (35)

[[illegible]]

decoder

double register

Progressor

coder

g

Aggregator

[[NB04-079]]

Marker

Progressor

Digits doubler

Aggregator

[[DIAGRAM]]

[[NB04-080]]

19-1-50

Since making the last diary note in this book “much water has flowed”
All the decoding arrangements for store selection have been tested and found to work satisfactorily (after rejecting about 8 storage units)
~~And~~ A programme ~~h~~ which put ~~a~~ 32 different numbers into each tank (14 being used) ie 32x14 numbers and then transferring them out again has been successfully performed
That was completed on Wednesday. Thursday morning was spent checking up on

multiplication after last Saturdays modifications and a Tank failure (mier).
On Thursday afternoon the assault on Output was started only to find that the Teleprinter would not satisfactorily produce end pulses. There were two faults
(a) Occasionally two end pulses were produced
(b) Occasionally no end pulses were produced
After examining the circuit it was decided that an unsatisfactory relay arrangement was being used to produce

[[NB04-081]]
the end pulses and after making a temporary modification the extra pulses were eliminated.
The lack of end pulses was not so easily cured until (by logic) it was found that the lengthened pulses that were being used to reset the EP flip flop ~~could~~ were the cause of the trouble. Roughly the circuit was :-

[[DIAGRAM]]

the resetting of the ff at D_{35} permitted a D_0 to pass thro ~~the~~ a gate

Unfortunately the lengthened pulse was occasionally being chopped by the relay so that the tail end of it was getting thro the relay contacts & reset the flip flop on - not D_{35} but possibly D_1 :-

[[DIAGRAM]]

so that D_0 was not able to get thro. Removing the lengthways condenser cured this.
Passing on to actual printing of characters by the teleprinter the programme

[[NB04-082]]

0	letter A
1	O_0

2 E_1
was used to produce a sequence which should ~~pro~~ cause the teleprinter to print "A." until further notice.
This worked spasmodically with the programme occasionally failing to step on from the O order and occasionally stepping on past the E order in spite of a clear accumulator.

There are certain points that have been glossed over in the attempt to produce something that works, and these will have to receive attention sooner or later.
They are.
1. General Attenuator tests in Computer
2. Amplitude of D_h pulse to TCT
3. " " " R_2 EP ex D_9.
4. " " D_{VN}

[[NB04-083]]

Programme for Monday 22-1-51

Proceed with Print Programme I using different characters but trying to find why programme stops.
Possible Avenues.
(a) count Mechanical EPs.
There should be 1 for each character printed after first set up.
(b)

There are two possible faults

(a) Failure [[on]] Output order
(b) Stepping on from E order.
If (a) then query
1. If order is still in Order tank, then there as been no coincidence in Stage 2. W_{12} will remain set and W_{13} reset.
2. If order tank is clear and SCT still has E_1 in it. W_{13} should be set. If it isnt then amplifier in [[LCN]] producing R_2 EP is probably at fault.
3.

[[NB04-084]]
(b) If stepping on from E order investigate
1. Accumulator is it negative
2. Examine R_2 EP produced by D_9 is it breaking thro gate in LC II.
3. Examine W_{14} is it being reset regularly
4. Examine D_9 is it large [[illegible]] to set f_4

22-1-51

Pulse Techniques.
F C Williams - Waveforms.

Triodes - out
Diodes & Pentodes with feedback

Uses:-

1. Radar
(a) Suppress Receiver
(b) Fire Transmitter
" ~~stray~~ TB
(c) Enliven Receiver
(d) [[Timebang]]
(e) Gate
(f)
(g) end & blackout
(h) repeat.

Trigger

Suppressor

TB
Brighten
Fast TB
Bright
gate

[[NB04-085]]

[[DIAGRAM]]

Uses: Electronic Computers
brief outline of principles.

What could Babbage have used in place of waveform generator
(a) camshaft.

(b) Servo mechanism

Handle angle Difference Amp Motor Gear Angle
~~Driver~~

[[DIAGRAM]]

Comparison of Triode & Pentode pulse producing circuits.

[[DIAGRAM]]

[[NB04-086]]
Amplitude Width &
determined by valve characteristics
component valves

[[DIAGRAM]]

[[DIAGRAM]]
line of coalescence

Poor load line
good load line

Effects

Amplitude		Duration	
Triode	Pentode	Triode	Pentode
R_2		R_3	R_3
V_2 I_a V_g	None	C	C
V_2 I_g V_g		V_1	
R_3 small		R_1	
[[load.]]	Impedance at a [[>]] 2K		

[[NB04-087]]

Feedback

[[DIAGRAM]]

See Saw

virtual earth at grid.

Velodyne

22-1-51

Progress on Output

Quite good progress
The programme produced by Hemy which prints 9 characters first is one case and then in another works OK (I think) as far as the computer is concerned.
There have been a few "corruptions" which I feel are due to circuit design. ~~The Output Units containing~~ the valves supplying relays are causing rather horrible bumps on the HT line which are detrimental to other circuits eg gates on the same unit and

[[NB04-088]]
it seems that it will be necessary to supply these from a separate source.
If there are only 5 valves which are ~~supplying~~ needed to be supplied in this way it may be possible to use an auxiliary supply for these for testing pending a more acceptable solution.

25-1-51

The corruptions on the Output sequence were eventually traced to a fault on the teleprinter
Gibbs produced a mod in about 2 hours work & after that the whole programme worked satisfactorily
The programme printed 9 characters first as letters and then as numbers and all

combinations were tested satisfactorily.
Work is now proceeding on the Starter and although things looked a bit glum for most of yesterday
there was a bright spot just after 6pm when I traced the source of some extra end pulses to an un"[[squerched]]" contacts

[[NB04-089]]
As things stand at present all the end pulses are being received and added into the sequence control tank but the Initial orders themselves are not being ~~produced~~ put into the store. I have not worried about this as yet as it would seem to be due to some simple fault which can easily be remedied.
During the setting up of the starter there have been two faults
(a) spasmodic addition of “1” into SCT.
This was found to be due to interaction of two relays a & θ working in series. Relay a

is now redundant and by shorting it out and [[squerching]] θ this trouble was removed.
(b) Additional EPs going into SCT. This was not so easily found as conditions appeared to be varying so much. There were many signs of interference due to sparking on many inputs but most of this was eventually found to be due to leads going to the Cossor. It is fatal I find to try to Synch a scope on a lead ~~being~~ connected directly to relay contacts.
Eventually by elimination

[[NB04-090]]
it was found that [[squerching]] the Uniselector contact doing the EP breaks solves the problem.
Fortunately one or two spare [[squerch]] circuits have been provided in the Starter unit and it has been simple to just hook one in here & there ~~to try~~

26-1-51

I was wrong about the one simple fault that prevented the initial orders from getting to the store. There were three!
After getting the initial orders in and curing a couple of corruptions in the digits due to fault in wiring to [[plessey]] plug I am left with two problems one at least of which must be solved somehow.
The first which took so much time yesterday and which is still not resolved is that in stepping from 43 to 44 contact on the uniselector W_{13} resets without any 1 going

[[NB04-091]]
to the SCT ~~and~~ without setting W_{12}. In fact this does not cause any trouble as there is no legitimate stage II in the II sequence. At the same time it is rather disturbing not to be able to find the cause of this.
The second fault which has not yet been considered at all is the appearance of 1’s in the D_0 & D_{18} positions of the store. These are transferred liberally around the machine ~~by~~ presumably by the spikes at the end of the coincidence waveform ~~and~~ on unselected

input & output gates. At first sight these would not appear to be very serious as the

D_0 & D_{18} positions are cleared whenever transfers are made of short numbers to & from the store. There is a possibility however of using two short numbers as a long one and if D_{18}'s have crept in to the store they will have some significance in the long number transferred out.
This will have to be cleared in some way but for the time being I am ~~not~~ leaving this for a later date.

[[NB04-092]]

27-1-51

PS down
Tape Feed.
PS Up
PS Down
Tape feed.

[[DIAGRAM]]

Energising Pecker Solenoid withdraws peckers
Peckers must not be released until tape has moved on.
Releasing TFSol. moves on paper.
Paper must not be moved until peckers are withdrawn

[[DIAGRAM]]

Start

[[DIAGRAM]]

PS & TF energised together
TF released first by its own action in energising Q (PS must have made first to energise T
PS released by its own action in energising T which in turn energises R.

[[NB04-093]]
JMMP has produced a solution to the problem of resetting W_{13} during mechanical operations.
He proposes to make use of the order 00000 in the order tank [[dummy]] to produce a coder waveform which will produce a reset pulse

26-1-51

Dismantling D4.
Mercury - quite clean
Attenuator screw - normal.
P'end. (with [[~~geared~~]] bad saw cut
Obvious sign of leakage on [[crystal]]
no marks on electrode surface of significance
Rubber washer not stuck
Crystal apparently OK.

P end no apparent leakage

[[NB04-094]]

[[DIAGRAM]]

But if

Saturday Work

Investigate Mier Tank - faulty
PAD 3μS. ✓
R_2 EP Amplifier ✓
Pulse Wiring
Cleats on Jones Plugs

[[NB04-095]]

[[UPSIDE DOWN]]

Pot	25/10/
33/1	25
31/1	73
2	57
19/1	65
2	33
32/1	49
24/1	57
17/1	78
2	39
3	80
1/3/1	42
1/20/1	31
1/5/1	22
39/1	100
30/1	38
2	52
3	4

Pot	25/10/50
40/1	18
2	22
28/1	56
37/1	50
2	100
3	55
27/1	40
34/1	50
34/2	17
22/1	36
22/2	33
23/1	57
2	40
1/22/1	35
1/8/1	30
16/6/1	23
16/06/2	35

Pot	21/11/50
16/4/1	37
2	44
Freq Cont	
4/1	90
2	26
[[Coder]]	15
2/2/1	25
2	100
3	47
4	47
5	50
6	40
11/1	~~21~~ 48
2	51
12/1	51
2	35
9/1	
45/1	64
1/25/1	30
1/18/1	53
16/3/1	33
2	50
1/4/1	30
16/5/1	35
16/5/2	65
36/1	60
15/01/1	95
1/6/1	20
	20

[[LAST PAGE BLANK AND UPSIDE DOWN]]