[[NB05-001]]

[[CIRCUIT DIAGRAM]]

29-1-51

Pulse Techniques

Mr Rose - Mathematical Treatment

Input [[square wave]] R L series

$$E = R_i + L\, di/dt$$
$$di/dt + R_i/L = E/L$$

$D = d/dt$

$$(D + R/L)i = E/L$$

if character
$i = Ae^{-Rt/L}$
is solution

Particular integral = $E/L\ L/R = E/R$

$$i = Ae^{-R/Lt} + E/R$$

is $i = 0$ when $t = 0$.

$$0 = A + E/R$$
$$A = - E/R$$

[[NB05-002]]

$$\therefore i = E/R(1 - e^{-R/Lt})$$

$$e^x = 1 + x + x^2/L^2 + ...$$
$$e^x = 1 - x + x^2/L^2 -$$
$$1 - e^x = x - x^2/L^2 - ...$$

$$\therefore (1 - e^{-R/Lt}) = Rt/L - (Rt/L)^2/L^2 ...$$

if Rt/L is small .....
time constant L/R

3 cases to be considered
(a) before time constant
(b) at " "
(c) after " "

From time 0 to t_0

$i = E/R(1 - e^{-R/Lt})$
$V_R = E(1 - e^{-R/Lt})$
$V_L = Ldi/dt = LE/R(0 + R/Le^{-R/Lt}) = Ee^{-R/Lt})$

Removing Voltage
at t_0 $i = E/R(1 - e^{-R/Lt0})$
at t_0 voltage = 0
∴ new equations $(D + R/L)\, i = 0$
$i = Be^{-R/Lt}$
At t_0 , $i = E/R(1 - e^{-R/Lt0}$
∴ $E/R(\ldots) \text{ s } Be^{-Rt/L}$
$B = E/R(1 - e^{-R/Lt0})e^{-R/Lt0}$
From t_0 onwards $i = E/R(1 - e^{-R/Lt0})e^{R/Lt0} \times e^{-R/Lt}$ $E/R(1 - e^{-R/Lt0})e^{R/Lt0}e^{-R/Lt}$
$= E/R(1 - e^{-R/Lt0})e^{-R/L(t - t0)}$
$V_R = R_i$
$V_L = LE/R(1 - e^{-R/Lt0}) \times -R/Le^{-R/L(t-t0)}$
$= -E(1 - e^{-R/Lt0})e^{-R/L(t-t0)}$

[[NB05-003]]
<u>Rc series</u>

$E = Ri + 1/c \int i\, dt$
$0 = Rdi/dc + 1/ci$
$(D + 1/Rc)i = 0$
∴ $i = Ae^{-1/Rct}$ $i = E/R$ when $t = 0$
$V_{Rs} = Ee^{-1/Rct}$ $E/R = Ae^0$
$V_R + V_c = E$ $A = E/R$
∴ $V_c = E(1 - e^{-1/Rct})$ $i = E/Re^{-1/Rct}$

(note similarity to V_L)
From t_0 -->
Remainder follows similarly to
Inductance -->

$(D + 1/Rc)i = 0$
$i = Be^{-1/Rct}$

Producing -->
$V_R = Ri$

$i = E/R(e^{-1/Rct0} - 1)e^{-1/Rc(t-t0)}$

$V_R = E(\quad)$
$V_c = -E(e^{-1/Rct0} - 1)e^{-1/Rc(t-t0)}$

<u>Power</u>
From time 0 to t_0

Generator $E^2/Re^{-1/Rct}$

Resistance $L^{s2}/Re^{-2/Rct}$

Capacitor $E^2/R(1 - e^{-t/Rc})e^{-1/Rct}$
$=E/R(e^{-1/Rct} - e^{-2/Rct})$

Max value can be found by differentiating & equating to zero.

[[NB05-004]]

From t_0 ----------> (PONER)

Generator ---------- 0
Resistance $E^2/R(e^{-1/Rct0} - 1)^2e^{-2/Rc(t-t0)}$

Capacitor = - Resistance

Energy $\int$ Power *dt*
0 to t_0
Generator $= E^2/R \times - Rce^{-1/Rct} + K$

at t = 0 Energy = 0 .

$0 = -CE^2e^0 + K$
$K = CE^2$

Energy $= CE^2(1 - e^{-1/Rct})$

From t_0

Energy Generator = 0

~~Resistance $-E^2C/2[(e^{-1/Rct0} - 1)$~~

Resistance $-E^2C/2[(e^{-1/Rct0} - 1)e^{-2/Rc(t-t0)} + 2(e^{-t/Rc} - 1)$

[[NB05-005]]

E [[CIRCUIT DIAGRAM]]

$R_2i_{R2} = q_c/C$ $i_c = dq_c/dt$

$i = iR_2 + i_c$ $\therefore$ $E = i_{R2}R_1 + i_cR_1 + q_c/C$

$i_{R2} = q_c/CR_2$

$E = q_c/CR_2 R_1 + dq_c/dt R_1 + q_c/C$

$R_1 dq_c/dt + R_1+R_2/CR_2\ q_c = E$

mult thro by

$R_1R_2 / R_1+R_2\ dq_c/dt + q_cC = ER_2/R_1+R_2$

i.e. reduced to normal form with *q* in place
of *i* and R_1R_2 / R_1+R_2 in place of *R*.

30-1-51

After quite good progress last week with seemingly only a few hours work between me and completion of the Input system (Tape Reader) yesterday was a real head [[ache]].
On Saturday a couple of mods were made and tested, but after a brief [[positive]] test on the Coord, I jumped to Input & everything was wrong It was not long before I was back on the coord with a simple AUE programmed failing to work. Eventually I was forced to the conclusion that the mod on the coord

[[NB05-006]]
to amplify the R_2 EP was the cause of the trouble. Having cut this out, it still would not work. It was an hour later that I found that my programme had slipped in the memory. Reinserting the programme showed OK for no amplifier and with the amplifier back there was no success so I was forced to the conclusion that there must be a "[[sing]]" of R_2 pulses round when the gain of the loop > 1. Reducing gain of amplifier (Designed to be fixed gain) solve the problem but I must go back thro this circuit

when doing attenuator checks.
Returning to ŧ Input there is still trouble from this. It is a fundamentally bad arrangement of relays with spark quenching condensers causing HS relays to make momentarily. Among other troubles ~~the~~ more than one EP is being received for each input order.
A visit today from Mr Foster of Elect Eng. re articles. He was very impressed with the raster scope and generally with our whole set up.

[[NB05-007]]
JP informs me that the fee they offer for my article is 6 guineas which I consider very easy money.

30-1-51

Good progress again.
After triggering the tape reader to operate more reliably the Input Sequence (I.E) seemed to work OK so using ~~the~~ a spare punched tape & connecting up the tape reader, & starter, ~~and Teleprinter~~ we held our breaths & pushed the button.
This produced rather satisfactory results as the Tape reader started up as the Starter came to rest and concocted an amazing variety of numbers in store position 0 but obviously was not getting anywhere.

[[NB05-008]]
By stepping round the sequence in single steps it was soon apparent that the trouble was that the information on the tape being used was not suitable as there were no D's & I^5's etc to indicate the end of a number.
A call on Hemy for more programme produced an incomplete tape which it was claimed would cause the Printer to execute A B C D E etc as each part of the initial order was executed. We crossed our fingers and connected up the Teleprinter.

When the button was pressed the reader read and the printer printed - but unfortunately not what was required.
In fact after several starts it had printed as many different versions and come to a halt after trying to execute and impossible order.
We tried stepping the program on slowly but this was such a tedious program that when it eventually went wrong it was because Gibbs had jogged the SPS to such an extend that the contents of the accumulator disappeared.

[[NB05-009]]
The rather wonderful thing is the fact that we have got everything connected up together and it is doing things - not always the right things but it is doing so much right that it is very promising and hopeful.
The one point to hang on to is that LEO has taken in a programme and printed a result.

LEO has spoken.

It is extremely tedious to check that each order ~~pe~~ stepped on by manual control

~~does~~ has the required effect and I think that a much simpler programme is called for ~~e~~. In the more complicated programme it would help enormously to have an idea of what the accumulator should hold at each step.

[[NB05-010]]

31-1-51

Required
(a) Copy of Initial Orders with description of effects.
(b) Condition for manual single step with much less triggering.
(c) Simpler programme with accompanying indications for what to expect in the acc

(a) & (c) should be supplied by Hemy & Co. I must provide for (b) myself.

Requirement for Manual Single step etc.

(a) Mix Number simulator & Input ~~/Ou~~ digits before going to Transfer Unit.
(b) Inhibit EP to occur after starter sequence.
(c) Starter D_9 to be inhibited
(d) SPG to be corrected via mixer to [[mich]] End Pulse line
(e) Inhibit EP to be brought to a "stop" Button

[[NB05-011]]
Building Policy.
It seems desirable that some of the operating controls should now be brought into effect so that the machine sequences ~~b~~ can be brought to a halt readily and stepped on at will.
In view of this I think it would be a good idea to forget the programme that cannot be done correctly for a while and to concentrate on manual control.
In the meanwhile Hemy should produce some simple tapes ie loops which

will test initial orders in easy stages.

[[NB05-012]]

31-1-51

Compositor

Answer in Aggregator

Functions
(1) Record number on mag tape in LEO code
(2) Register number and compositor instructions handed on by Reconverter
(3) Control Tape machine

Reconverter

Aggregator Decoder

Compositor

LEO REGISTER Composition Control

Composition

Number itself ----------> Decimal or Binary
(if decimal number of places up to 3
Common Colours Dec Point
Minus Sign
Suppression of non significant zeros
spaces & colours.

[[NB05-013]]

Main Parts of Compositor

0. LEO Register
1. Composition Control - receive coded instruction from decoder (recoverter)
2. Composition Distributer
deals with tabulation information

	(Prefixes & suffixes)
3. Number Distributer	
	Pick off digits from LEO Register and interpolated common colours & dec points
4 Output Reader	Monitors numbers picked off for recording on tape
5. LEO Code Transmitter	
	feed the elements of the teleprinter signal to the tape Machine
6. Time scale	
	Divides 5 Kc/s by 5 and 8 to give 8 ms

31-1-51

Not much progress today although I think I have a clue. Hemy has produced a simpler programme today but before going on to that I have been doing some tests on straight forward input synthesising with a ŧ view to getting more knowledge of the Starter Sequence and how it works.
It has not been convenient to use much of the Operating Control owing to the fact that it calls for some mods on a very overcrowded unit.

[[NB05-014]]
In its place I am using a couple of switches on my table and an external connection to the flipping circuit to give me varying speeds of operation.
Out of my tests arises the fact that generally on low speeds the computer works satisfactorily, at machine speeds it fails, but usually on an order in position 22 of the store which it is found has been changed or lost
Now the sequence dealing with the order says :-

22 T_{40}
23 A_{22}

ie position 22 is used twice in quick succession and this is the only thing that suggests itself as a cause of failure. If a circuit used in the selection of store position 22 has a slow ~~ret~~ recovery time for some reason, it may not be ready for use when called on the second time.
In order to test this I devised a programme :-

0 T_6	which simulates the conditions imposed in
1 A_0	Starter sequence and behold - it fails with the
2 A_5	order
3 T_0	
4 T_0	
5 D_{20}	

[[NB05-015]]
in position 0 cleared.
An attempt to trace the cause of this with a second programme was not productive ~~but~~ apart from showing a marked difference between numbers going to the transfer unit ex store and ex computer. Those coming from the store being much the smaller.

This must be investigated tomorrow.
I feel that this is a secondary point however and I want a simple programme that will do the T. A sequence and while giving indication

of any change in the order in the first position will not ruin the programme as a result
Possible programme is :-

0	0	T_0	= 11011	start on 1.
	1	T_8		clears Acc
1	2	A_1		T - T = 0
	3	A_0		
2	4	$T_{9 \to 10}$		0 ----> 10
	5	A_9		T_8 - Acc
3	6	T_1		Transfer to 1
	7	E_1		Control to 1
4	8	∓ Holds zero always		
	9	T_8		

Inspect position 10, this should always be 8 with no digits in order position

[[NB05-016]]
if order in position 1 is changed by reason of slow recovery time as suggested above then something other than 8 will appear in position 10. In any case the T8 should be replaced before the loop is completed.
When changing is noted in Store position 10 then contents of store position 1 and particularly input output & clear gates should be watched carefully.

1-2-50

The framework of the control desk is now in its place and awaiting the various units which are required for it. At present the teleprinter tape reader and starter are operating in a [[lashup]] form on two tables at the end of the racks. Several construction jobs are still outstanding.
The additional racks for extended store and the Annexe system are here and waiting to be put into position but this will cause a major upheaval as the false floor on the outside of the Computer will have to come

[[NB05-017]]
up and also some extra trunking for two additional

1-2-50

The fault described earlier persists and it seems to be one of the worst yet with many peculiar facets to it.
The programme mentioned has been used today and although at first there was no evidence of odd digits being transferred to position 10 There was other evidence that all was not well.
It was not possible to get a clean locked picture of the Stage II waveforms that could be used to compare various gating waveforms and when the output digits coming from the

[[NB05-018]]

store were examined on the raster scope it seemed that the programme was being short circuited in some way as not all of the orders were being called out. A phenomenon which has not yet been explained was causing the brilliance of the digits of the orders being called out to vary at a very slow rate, as if the period of the programme was in some way beating with the mains.
Ignoring this effect for the time being attention was turned to the number

being transferred to and from the store
It was immediately apparent that the pulses from the store were of considerably less amplitude than those from the computer. If the gain of the amplifier in the Transfer Unit was reduced then the digits in position 10 of the store showed that in fact the order in position 1 was being changed as [[expected]] With the gain at optimum however There was no visible corruption although the programme was still going wrong. The transfer unit was taken out and the amplifier modified to

[[NB05-019]]
give reasonable results from an input of 10 volts
With the ~~gain~~ Transfer Unit back in position the pulses from store were quite satisfactory but the programme still was wrong.
At no point in the path of numbers between accumulator and the store could I find any signs of corruption.
I thought I had a clue late this evening when I looked at the T coder waveform It was apparent that this was not correct. There should be three of these

and one of which was likely to be of long duration.
It seemed possible that if one was particularly long it might be suffering from faulty time constant or zero restoration in some circuits.
Examining these waveforms showed that while there was an occasional extra long one it was by no means one in three and even this was not being badly treated anywhere.
In examining the gating waveforms more closely I noticed that there was a slow change in amplitude of some of them which was in step with the changing of the programme I eventually traced the source of

[[NB05-020]]
this to the C_{17} waveform produced in the Coder. I suspected heater cathode leak but changing appropriate valves did not cure some.
Later
This effect has been shown ~~to no~~ to be due to a beat with mains and is not believed to be detrimental.

Query LC28 is there a need for a delay in C_1 in order to gate R_2 - is W_6 being produced reliably
No because the EP shutting off C_1 is at least 2m/c after R_2

The Ideal Computer

Order. Clearing Accumulator
A.T.
Pruning waiting time

3-2-51

Still no [[more]] progress on the problem of the day
A simple programme

0	G_0
1	T_{40}
2	A_1
3	A_0
4	E_1

Works without fault but a similar sequence in the Starter orders eventually loses the T_{40} order

[[NB05-021]]
The effect is that the program proceeds until it is required to carry out order No 22 and on referring to it it has either been modified in some way so that it cannot be carried out as an order or else ~~it~~ the store position is completely clear.

Order Clearing Acc
~~Two alternatives~~
~~(a) Use new order mixed with T to produce C_{20} to produce W_9~~
~~(a) New coder waveform gates a D_0 to set W_9 flip flop which is reset by the next flip fl D_0 the gated reset pulse is also used to as end pulse. Also revision of present clearing system~~

~~[[DIGRAM]]~~

[[NB05-022]]
New Coder waveform C_x±

C_x- to Acc Clear
W_9

C_x+ d E.P.
D_0

AT order to give add from and transfer to a single store position in same order.
Required New Coder waveform + and - All normal coders for Add
Add EP is diverted and stimulates coince unit a second time ~~by ga~~

Diversion of Add EP is by two gates controlled by C_y ± negative inhibits EP positive passes EP to coince unit where it is mixed with normal stim pulse. This stim pulse also sets a new flip flop W_2 positive output of which is mixed with C_{20} to give W_9 and with C_{19} to give no out to ~~transfer~~ Acc [[10]] unit
It also goes to coder where it is mixed with ITU to give C_{17}±
An EP to the AT order was the ~~reset~~ pulse that resets W_9 gated with W_2

[[NB05-023]]
[[SIDEWAYS DIAGRAM]]

Add EP g to EP mixer

C_y ∓ to R_1 & R_2 gate in Coince Unit 1

Add EP g to Coince unit as stim pulse

W_2
f to LC 34 mix with C_{20} for W_9

to coder to produce C_{17} ±

~~to R_1 & R_2 gate~~

g A T E P

Reset W_9 pulse
from LC 34

d

Further thoughts on present problem have not bourne fruit. It seems likely that the fault is due to a corruption which occurs during either a T or an A order and unless a short programme ~~using a single order~~ can be made to reproduce the fault it is difficult to find a way of tackling it as in the real programme only one fault is needed to stop it. A possible way of doing it is to set up A_x on the number simulator so that every stage 2 carries out that order and the order cannot be changed. Then look around

[[NB05-024]]
the normal paths. It must be remembered that the number x simulator will be around too so that a double picture should be looked for

<u>Component Parts</u>
a Input System
b Output System
c Tape Box
d Set of Alarms.

<u>Tape Machine</u>

<u>Uses</u>
1. Initial Recording of Data — Normal Speed 50 Bands

2. Checking of Data
Collater — 50 Bands

3. Feed Converter
Converter Annexe

4. Recording of Result I — 333 Bands
Annexe Recom Compos
1000 Bands

5. Print Results — 50 -

[[NB05-025]]
6 Separating Results Separator

7 Blending of Results Blender

8 Amending Permanent Data

333

Amender

Tape Positioning
1. Before recording from teleprinter ensure sufficient tape for recorder
Clean "nose"
2 After Recording introduce a clean "tail" to provide sufficient separation between record head and end of information
3 After checking introduce clean tail as ~~will~~ before

5-2-51

Pulse Techniques

Mr Rose Mathematical Treatment II

Response to $\sin^2$ wave

[[$\sin^2$ DIAGRAM]]

$E\sin^2 pt$

$L di/dt + Ri = E\sin^2 pt$

$(D + R/L)i = E/2L(1 - \cos 2pt$

$i_c = Ae^{-R/Lt}$

complementary ~~$D^2 = -4pt$~~

Part integ 1 = $E/2L \div R/L = E/2R$

Part integ 2 = $E/2L \cos 2pt / D + R/L = E/2L \,.\, D - R/L\cos 2pt / D^2 - R^2/L^2$

$= E/2L\ (-2p \sin^2 pt - R/L \cos 2pt \ / \ (-4p^2 - R^2/L^2)$

[[NB05-026]]
$z = \cos 2pt$
$D_z = -2p\sin 2pt$
$D^2 z = -4p^2\cos 2pt$
$= -4p^2 z$
$D^2 = -4p^2$

$= E/2L(2pL\sin 2pt - R\cos 2pt / 4p^2L^2 + R^2)$

$i = Ae^{-R/Lt} + C/2R - E/2L$ { }

repeat for t_0 onwards
result very similar to sine wave output :-

[[DIAGRAM]]

To eliminate a pulse from Dc supply

[[CIRCUIT DIAGRAM]]

$q_C/C = Ri_R$

$q_C = CRi_R$

$E \quad R_1(i_R + i_C) + R_L(i_R + i_C) + Ri_R$

$i_C = dq_C/dt = CRdi_R/dt$

$E = R_1(i_R + CRdi_R/dt) + R_Li_R + R_LCRdi_R/dt + Ri_R$

$E = (R_1 + R_L)CRdi_R/dt + (R_1 + R + R_L)i_R$

$L = (R_1 + R_L)CR$

[[NB05-027]]
Series R. L. C.

$E = R_i + Ldi/dt + q/C$

$dE/dt = Rdi/dt + Ld^2i/dt^2 + i/C$

When E is constant $dE/dt = 0$

$Ld^2i/dt^2 + Rdi/dt + i/C = 0$

$E = Ld^2q/dt^2 + Rdq/dt + q/C$

Particular integral $C\,E$

To solve $Ld^2q/dt^2 + Rdq/dt + q/C = 0$

$(D^2 + R/LD + 1/LC)q = 0$

Write this as

$(D - \lambda_1)(D - \lambda_2)q = 0$

Where λ_1 & λ_2 are roots of equation

$\lambda^2 + a\lambda + b = 0$

~~d~~ . $a = R/L$

$b = 1/LC$

Three possibilities

1. $a^2 - 4b > 0$
2. $a^2 - 4b = 0$
3. $a^2 - 4b < 0$

Case 1.
λ_1 & λ_2 are real and unequal
2. λ_1 & λ_2 " " " equal
3. λ_1 & λ_2 " complex and unequal

Case 1. $q = Ae^{\lambda_1 t} + Be^{\lambda_2 t}$
2. $q = (A + Bt)e^{\lambda_1 t}$
3. $q = e^{-a/2t}(A\sin\sqrt{4b - a^2/2}\, t + B\cos\sqrt{4b - a^2/2}\, t)$

1 overdamped
2 critically damped
3 oscillation

[[NB05-028]]
Long Pulse

Capacitance

Overdamped.

[[DIAGRAM]]

Oscillatory

[[DIAGRAM]]

Critically
Damped.

[[DIAGRAM]]

Inductance

[[NB05-029]]

[[CIRCUIT DIAGRAM]]

$R_{iR} = q_C/C \qquad i_R = q_C/RC$

$E = R_1(i_R + i_C) + L\, di_R/dt + L\, di_C/dt + q_C/C$
$= R_1\, q_C/R_C + R_1\, dq_C/dt + L\, dq_C/dt + L\, d^2q/dt^2 + q_C/C$

$= L\, d^2q/dt^2 + (L/RC + R_1)\, dq_C/dt + (R_1/RC + 1/C)q_C + (R_1 + R / R)(q_C/C)$

$E\ R/R_1 + R$
~~$E\ (R_1 + R) / R$~~ $= LR/R_1 + R\ \ d^2q/dt + L + R_1RC\ /\ (R_1 + R)C\ dq_C/dt + q_C/C$

if last term is negative system cannot oscillate

Fourier Analysis

Spectrum

$W(t) = a_0/2 + \sum a_n \cos n2\pi ft + \sum b_n \sin n2\pi ft$

$a_n = 2 / 1 / f \int_0^{1/f} W(t) \cos n2\pi ft$

$= 2f \int_0^{1/f} W(t) \cos n2\pi ft$

$a_3 \cos 3\theta + b_3 \sin 3\theta$
$= c_0 \quad c_3 \cos(3\theta - \phi$
where $\phi = \tan a_3/b_3$

[[NB05-030]]

[[SQUARE WAVE DIAGRAM]]

$a_0/2 = At_0f$

$a_n = 2f \int_{-t0/2}^{t0/2} A\cos n2\pi ft\ dt$
$= 2fA/2\pi fn\ (\sin n2\pi ft)_{-t0/2}^{t0/2}$

$A/\pi n(\sin n2\pi ft_0 / 2 + \sin n2\pi ft_0 / 2\ )$
$2A/\pi n(\sin n\pi ft_0)$

~~$n\pi ft_0$~~ $2A/\pi n\ \sin n\pi ft_0 / n\pi ft_0$

$2Aft_0 \qquad \sin X / X$

Plot $\sin X / X$

let $1/f \div t_0 = k$

then $a_n = 2Aft_0 \sin X / X$

$a_n / ft_0 = 2A\sin n\pi ft_0 / n\pi ft_0$

but $ft_0 = 1 / k$

$a_nk = 2Afn/k$

Amplitude spectrum $k = 2$

$k = 1 / f \div t_0$
a_n coeff of $\cos n2\pi ft$

[[NB05-031]]

$k = 4$

[[WAVEFORM DIAGRAM]]

as $k \to \infty$ envelope becomes continuous

[[WAVEFORM DIAGRAM]]

if

$W(t) = \int_0^\infty a_\omega \cos \omega t \, d\omega$

~~$a\omega$~~ $a_\omega = 1/2\pi \int_{-t0/2}^{t0/2} W(t) \cos \omega t \, dt$

$= 1/2\pi \int A \cos \omega t \, dt = A/2\pi \, (2 \sin \omega t_0/2)$

[[NB05-032]]

8 -2-51

A small amount of progress today but it is too early to say whether a solution has been found to my particular problem. After making tests on simple Add and Transfer programmes without a failure I put in a programme which was as near as possible a copy of that part of the Starter sequence that was failing. It failed with E33 in the SCT
now the sequence should never have produced a 33 at all so that I repeated the programme again and again until I found that the cause was

incorrect addition of 1 in 16 SCT. One of the orders was E34 ie 0001100…010
When the 1 was added to this, the carry failed so that the result was 0001100——001
As there was no order in the SCT the machine stopped here.
I o found that by reducing the amplitude of the 1 to SCT (operating amplifier gain in LCII) A reliable sequence resulted.
This caused attention to be directed towards the R_2 pulse loop, and eventually to EPs in general. One thing that I found was that there was

[[NB05-033]]
some splurge coming in from the Starter EP line. This was eventually traced to sparks on the HT & 50 volt line.
The cause of the particular spark annoying at this stage was the ~~V rela~~ pecker contact whose effect was being reversed by the V relay. ~~Sup Guit~~ Quite a considerable spark was found here and on suppressing this contact the trouble appeared to have disappeared.
A second disquieting discovery was that the 1 to SCT was varying in amplitude but this could be overcome by

increasing the gain again on the amplifier in LC II. After doing this, the original

programme was tried but it failed with the machine going into a closed sequence not including an I order. This was due as before to the order in position 22 being changed.
TRT has produced a programme which uses the Starter sequence without modifying any of the orders but I feel I should go back to the SCT 1 before going on to this

[[NB05-034]]
I must also examine the Starter orders to see if the effect of changing the order in position 22 could be caused by an error in the SCT counting.

Re the proposed AT order a snag not forseen is to prevent R_2 from first coincidence from starting up a new stage 1. This can be avoided by taking C_y - to the gate producing $R_1 + R_2$ then inhibiting $R_1 + R_2$ during the whole of the stage 2
The next sequence will

be started by the new endpulse.

---

0 T_0	14 S_{39}	28 E_8
1 E_{20}	15 E_{17}	29 A_{42}
2 P_1	16 S_7	30 A_{40}
3 U_2	17 A_{35}	31 E_{25}
4 A_{39}	18 T_{20}	32 A_{22}
5 R_4	19 A_0	33 T_{42}
6 V_0	20 H_8	34 $I_{40}D$
7 L_8	21 A_{40}	35 $A_{40}D$
8 T_0	22 T_{43}	36 R16
9 I_1	23 A_{22}	37 $T_{40}D$
10 A_1	24 A_2	38 E_8
11 S_{39}	25 T_{22}	39 P_5D
12 G_4	26 E_{34}	40 P_0D
13 L_0D	27 A_{43}	

[[NB05-035]]

6-2-51

More trouble on same circuits.
The SCT Half adder was found to be not working today due to changing characteristics of an SP61 & a low bias voltage. Correcting the bias voltage cured the trouble but it wasted much time. After many attempts to diagnose the trouble again I returned to my extract of the initial input orders and managed to show that the reader was causing at least some of the corruptions. This led to an assault on this piece of equipment - contacts & clearances being re set

I stayed this evening until 9 oclock playing with it but still in trouble.
The clearances on the pecker contacts need further adjustment on my experience as when the tape is forced well down onto its peckers same corruption still occur.
There is also some sparking on some of the contacts and I feel that this must be suppressed.

[[NB05-036]]

If ½ m/c is pruned off stage 1 & stage 2 does it mean a saving of more than ½ m/c on each stage?

0 Suppose under normal circs
16 an address is just missed by ½ m/c
32 then if that
48
64

	0	16	32	48	64	80	96
Coince		16		48		80	
	0	16	32	48	64	80	96

Suppose normal sequence takes ~~1m~~ 2mc

~~Seeking~~	2						
Stim	2½					Stim	2
~~See~~ Comp	2					Co	2
	4½		+ seeking time				4

0	16	32	48	64	80	96
	11½	11½	11½	11½		
	12					

1 in 32

7-2-51

It would seem that at last we are getting somewhere in this problem (Input). ~~After two~~ TRTs programme has been used by inputting by hand and this does a series of Adds & Transfers in various positions of the store quite adequately. Then by removing inhibition of EPs and preventing C23 from startup (~~order~~ ~~sequen~~ the reader the ~~starter~~ machine was made to perform on the starter sequence with varying patterns on the reader but without moving the tape or any associated relays. This worked without a hitch

[[NB05-037]]
almost proving that the fault still lay in the mechanism of the reader and its relays. Then when stepping on by single steps the W_1 waveform was noted to slip. Examination showed that this was in a marginal state and this was put right by substituting 22pf condensers for the 15pf used in the flip flop. In between each of these stages the Input programme was tried and <u>failed</u>. Then Hemys program stacking digits in store positions 45 to 63 was tried this worked all the way thro putting in all

combinations from 0 to 11111 in turn, but it was noted that occasionally not only the required digits were getting in but also ~~the~~ digits in a more significant position.
It has been left in Shaw & Gibbs hands to pursue this fault while I am at Cambridge tomorrow.
It seems obvious that a fault of this nature ~~which~~ would cause corruption of any

orders.
It is curious to note that these extra digits

[[NB05-038]]
appear to go into store position 40 when zero is being read and put in that position.
In the programme Hemy has put 0 as the first digit ~~of the~~ on the tape so that the starter sequences can treat the significant digits only [[in]] [[stacking]]
It would appear that a splurge may appear on the feed line during the time when the coincidence waveform of the input order is up.

JMMP on
Building a Computer 8-2-51

9-2-51
TRT JMMP EJK and self went to Cambridge yesterday. The mission was twofold.
(a) JP was giving a colloquium on "Building a Computer"
(b) We had some ideas which it would be nice to see incorporated in EDSAC Mark II. Dr Wilkes gave us some of the ideas which he hopes to incorporate in his new machine and his ideas were a little more than we bargained for to such an extent that

[[NB05-039]]
most of our suggestions seemed rather lame.
His main idea is to leave the logical design until last. His new machine will ~~be have~~ be a parallel one in all respects the store being a battery of 40 tubes each of which will hold one digit of each number.
The Arithmetic Unit and Control Unit will consist of registers (probably flip flops) ~~holding~~ each element of which will hold one digit of the number.
The control of the machine will be a crystal matrix

which will control entirely all the different functions. ~~in~~ Each function will merely organise the transfer of a number or order to and from particular registers of the machine in such a way that apart from the facility Add & Shift no functions will be built into the machine except in the Control matrix.
Dr Wilkes used the terms micro orders and micro programmes which ~~wh~~ will enable such a setup to be used in any conceivable way

[[NB05-040]]
It has the advantage that the Control may be considered as quite the last thing to be built, and in order to produce a machine of different characteristic it is merely necessary to rebuild the control.
It was also suggested that the control might be plug in so that the characteristics of the machine could be changed at will.
One idea which Dr Wilkes ~~sug~~ agreed to try was negative modulation in his storage units in order that automatic

gain control can be used.
The talk was well received although the discussion was at a pretty low level afterw[[ards]]. EDSAC has been behaving very well recently but a talk with Barton

afterwards showed that ~~it was might~~ all was not as will as might be. e.g. Half Adder trouble - the 1 to the counter tank needed to be amplified up to 18 volts!
We collected a tape reader and also four test programmes which should be very usefull

[[NB05-041]]
Gibbs & Shaw did not have much progress to report on Friday Morning. The story was one of retraced steps largely. Continuing the chase after the spurious digits that were being put into position 40 during or just after Input, after a days hard work it was found that during this pair of input add orders the digits were added into the accumulator. After a good deal of patient single stepping a digit was seen on the feed line during the add order.

While checking up on the Transfer ~~tank~~ Unit to see whether it was also on the discharge line JP noticed that one of the coaxial plugs was slightly loos (braiding clamp) and tightened it up. After this there was no further corruption The stacking of numbers programme now works without a hitch but often programmes involving output are still in trouble.
That a fault of this kind could have caused so much trouble is rather annoying but it does make a case ~~of~~ for more thought to be spent

[[NB05-042]]
on what kind of test can locate a fault of this kind.
Obviously a similar fault on any other storage unit but one of the transfer tanks would give a more permanent record ie ~~if it~~ as soon as ~~it a spark~~ a digit was produced it would be perpetuated ie it would continue to circulate and would do so under any circumstances until the tank was cleared.
[[In the]] transfer tank however such a pulse would be lost unless there happened to be a gate open at a cruxiel

moment so that the pulse so produced could be more permanently stored.

[[NB05-043]]

13-2-51

A great day today. LEO has not only spoken - he has spoken a mouthfull. Perhaps he has a little to learn on his presentation, but it is all very encouraging.
Hemys programme testing the Initial Orders has been carried out about 99% correctly. The results of them are to print

ABCDEPPGHPP

~~and~~ then to print all the initial orders
We had got as far as printing the first part several times but it was not until

Caminer had found a mistake in the last row of holes on the tape, and Land produced a new one, that Leo would complete the program It not only printed the initial orders but also printed the message :-

YOU SEE I CAN DO IT

This provoked a great deal of merriment but more was to follow.
Having ~~made~~ detected two small faults we decided to do it again and this time it went much more wrong. It printed every other initial

[[NB05-044]]
order - twice and at the end wrote
YOU SEE I CANA DO IT !
And they say that these machines cant think for themselves.
Yesterday and today have been full of hardwork, hope and failure. P & I worked till 10 oclock last night with very little to show for it but todays results have been worth it. There has been a great panic to get the machine working in time for the great visitation on

Thursday and it seems now that we will have something to show after all.

The fault that we thought had been eliminated last Friday was there again as large as life on Monday morning. Work today has proved my suspition that some splurge on the Feed line was causing these extra digits.
The trouble occurred mainly in the Transfer Unit where the discharge lines from Store, Input, & Computer

[[NB05-045]]
are mixed and amplified. With the legitimate pulses was some [[dash]] pulse breakthro end and any lifting of the baseline had the effect of putting these on a pedestal and as the amplifier followed by the two transfer Tanks were exceedingly sensitive (break thro of 3 volts being turned into full size pulses in some cases) it is not surprising that we had the trouble.
Todays work has been to provide a system which would ignore 7/8 volt pulses

but treat 10 volt pulses as full grown ones. This has not been done satisfactorily yet but so far so good.

14-2-51

There is much to be done today.
1. Clearing up & rechecking
2. Preparation of a routine for Tomorrow
3. Prepare alternative program in event of failure
4. Confirmation of yesterdays success
5. Laying out & wiring control panel

[[NB05-046]]
I think one of the first thing to be done is to go round the machine with a soldering iron fixing in some of the temporary hook ups & getting rid of as many crock clips as possible.
Then a general confirmation of yesterdays progress possibly with a little more research into the Transfer Unit.
Then, the positioning of the control panel and a gradual tidying up of the wiring of the machine in general e.g. it would be worth while to solder in temporarily the amplified

8 Buttons
4 Switches

Even D_0

Controls Required

(a)	Single Pulse ex SPG	Button
(b)	" " " Op Control	B
(c)	Starter Button	B
(d)	Clear Store Button	B
(e)	C_{17}±	S
(f)	Slow Speed.	S
(g)	Clear Acc	B
(h)	Clear SCT	B
(i)	Clear OT	B
(j)	Inhibit started D_9.	S
(k)	Reset W_{13} & PAD.	B
(l)	Inhibit EP.	S
(m)	Input/No Sim C/O	S

[[NB05-047]]

16-2-51

HRH was no more and no less impressed than I had expected. The information printed by the Teleprinter was unintelligible except of course for the message printed at the bottom which provided some light relief. Fortunately LEO made few mistakes - obviously not subject to stage fright and the Dem went off smoothly. A little more interest was shown I think in the interior of the machine when she saw the complexity of the circuits - "how many ~~of this~~ machines like these

in existance?" only one other in working condition - no others on commercial clerical problems.
This auspicious occasion called for an enormous improve in general tidyness of the lab and I must make an effort to preserve this. My own desk was clear for the occasion - the first time in months.
Work on the machine can go ahead again and I have been given a more or less free hand to proceed on which problem I deem the best tackled first. The object will be to bring the machine

[[NB05-048]]
to full operating condition as soon as possible so that Caminer & Co can get [[weaving]] on some of the programmes that they have kept up their sleeves for so long.
The first and most obvious fault to be cleared is the corruption in the Teleprinter which I Think are due to breakthro in the output Unit.
Other troubles to be cleared are occasional "1"s being added into the store. These have the effect of spoiling all of the test programmes

received from Cambridge

16-2-51

Small progress. Today I tackled the Teleprinter corruptions first of all & found them to be due mainly to a simple unwanted digit in the Output Unit. At first excessive breakthro was suspected but it was eventually shown to be due to the amplifier circuit feeding the relay valve.
By changing the valve I could ~~improve~~ reduce considerably the ~~cos~~ corruption but

the old & new valves had no measurable difference in characteristics

[[NB05-049]]
I have left this [[one]] point to discuss with JP on monday
Passing on to the reason for the failure of the Cambridge store test I find that it is due to the corruption of an order. The order calling out contents of a long store position to be added into the computor ~~becomes~~ either loses its long discrim digit or else refers to an odd store position. Either of these corruptions causes the clock pulses in the store positions to be transferred out as short

numbers and these therefore are not cleared by the addition of a D_1
This fault could also explain the trouble on the test programmes where initial orders are repeated twice.
A programme using similar orders was put in manually and functioned correctly, but it is quite likely that the corruption occurs when the orders are ~~tak~~ transferred to & from the accumulator when being adjusted I must produce a program which will do a similar job.

[[NB05-050]]

0	A_{4F}	T_{10D} to acc
1	A_{8F}	T_{12D} in acc
2	T_{4F}	T_{12D} to 4
3	S_{6D}	in acc
4	T_{10D}	
5	E_0	
6	D_{19}	
7		
8	D_{21}	
9		
10		

JP suspects that this error is possibly due to the coincidence waveform applied to the input & output gates not getting up early enough to catch

the D_1. I have yet to check on this but in view of the fact that cambridge manage to get away with it, it does not seem a likely theory. It would seem much more likely that D_{18}'s are being gated out by spikes resulting from Decoding as was experienced in the Action Decoding.

[[NB05-051]]

18-2-51

Second Thoughts on causes of corruption of Orders.
There seem to have been at least ~~three~~ two different forms of the corruption which causes the Cambridge Store Test to fail.
(a) 11…..1110101 corrupted to …..100
(b) 101 " " 111
~~(c)~~ In one case a digit has been lost, in the second case an extra digit has crept in. In the first case the order, ~~now~~ original referring to a long number, even [[compart]] has been changed to short number even compartment, In second case to

long number odd comp.

as the machine will not recognise the long no digits when dealing with an odd compartment, both cases result in a short number being transferred.
Now for extra digits to be added to compartments it is reasonable to assume that somewhere in the machine there are digits in the positions being let out onto Deed & Discharge buses.
In some cases they may be added to an original order, in others they may be mixed with it.

[[NB05-052]]
The resetting of Tank No SRs takes place at D_0 and is productive of spikes in the D_1 position while it has always been considered that these spikes occur outside of normal machine activity time it is a matter for concern that these spikes are applied equally to input and output gates of storage position.
Now the same spike ~~appl~~ occuring at D_1 time and being applied to an input gate and an output gate would cause the transfer of ~~any~~ a D_1 present in the second tank into the first

With D_9 end pulses occurring at D_{18} this could produce the same effects at D_{19} time. Whether the same sort of thing could occur at D_2 and D_{20} is not clear as a close examination of these spikes has not been made.

[[NB05-053]]

19-2-51

Pulse Techniques

Lecture ~~IV~~ V
Delaylines and Pulse Generators

Programme.

1. Introduction	I^5 C Williams
2 Passive Networks	Rose
3 " "	Rose
4 Valves	Neil
5 ~~Feedback~~ Delay lines & Pulse Gen	Wallace
6 ~~E.S. Time Bases~~ Feedback	
7 ES Time Bases	
8 EM " "	
9 H F Pulse Amp.	
10 " " "	
11 Analytical Methods	

(a) Delay Lines
1. Profile of travelling wave constant
2. Velocity "c" constant
3. Propagation in either direction

$v = f(x \pm ct)$

$t = 0$

$t = 1 / c$

Distributed Line

[[DIAGRAM]]

Distrib because capacity & inductance cannot be separated

L per unit length
C " " "

[[NB05-054]]
~~Inductance~~

$C = K / 1.8 \times 10^{12} \log_e D/d$ ~~henr~~ Farads per cm

$L = 2\mu \log_e D/d$ henries/cm

μ permeability $\approx$ unity

$c = \sqrt{1/LC}$ cm/sec

Example = $3x10^{10}/\sqrt{\mu k}$ cm sec

Propagation
$V/i = R_0 = \sqrt{L/C}$
between 30Ω & 100Ω

[[PULSE DIAGRAMS]]

If line is terminated by R_0 OK
" " " shorted
$V_t = 0$.
" " open
$i_t = 0$
example - open circuit

[[PULSE DIAGRAMS]]

[[NB05-055]]
at opencircuit
voltage reflected same sign
current - with change of sign

at closed circuit

voltage reflected with change of [[illegible]]
current - same sign

termination R_0 no reflection

Line shorted both ends

[[PULSE DIAGRAM]]

~~line shorted one end~~

Incorrectly terminated line

[[PULSE DIAGRAM]]

exponential damping.
Practical line
Conductors have resistors
(pulses attenuated)
Dielectric Loss.
c varies with frequency giving deterioration of shape.

Delay 1μS 200 yds

[[NB05-056]]
Practical Delay Lines
(a) Continuously Wound Delay Line

[[DIAGRAM]]

Inductance and Capacity increased
Balanced pair wound in opposite directions
Errors introduced by this type of line
[[illegible linkage?]] of turns caused [[limitation]] of rise time
Minimum rise time = $\tau \times D / L$
Can be improved by equalising intermittent capacitance padding

Lumped Delay Lines

[[DIAGRAM]]

$R_o \sim \sqrt{L/C}$
c
delay per secon ~ $n\sqrt{L/C}$
Cut off frequency = $\omega_c = 2 / \sqrt{L/C}$

miniumum rise time of τ / n

equalisation M helps
slightly analagous to

[[DIAGRAM]]

[[NB05-057]]
Pulse Generators

Soft ~~Pul~~ Valve discharge in C

[[CIRCUIT DIAGRAM]]
[[PULSE DIAGRAM]]

charge 680K x .01
discharge 440Ω x .01

[[WAVEFORM DIAGRAMS]]

[[CIRCUIT DIAGRAM]]
[[PULSE DIAGRAM]]

Replace C by delay line

[[CIRCUIT DIAGRAM]]

$i = V_0 / R_0$

[[NB05-058]]
[[CIRCUIT DIAGRAM]]

Charging Cycle.
[[CIRCUIT DIAGRAM]]
[[PULSE DIAGRAMS]]

[[PULSE DIAGRAMS]]

Increase repetition frequency

[[PULSE DIAGRAMS]]

as frequency increases rise becomes more linear
current becomes higher.

[[NB05-059]]
Blocking Osc

[[CIRCUIT DIAGRAM]]

Delayline for decoding

[[CIRCUT DIAGRAM]]

pair of pulses separation T will produce output

[[CIRCUIT DIAGRAM]]

[[NB05-060]]

20-2-51

A solution of sorts has been found for the teleprinter corruption With JP yesterday we found that the corruption was caused by interaction of ~~two~~ three faults.
(a) Amplification of Hum from HT line
(b) Breakthro of digit pulse in gate
(c) Pick up of voltage surges from relay valve by amplifier circuit
~~T~~
a & ~~b~~ c were dealt with satisfactorily and without them (b) is not harmful.
(a) was avoided by using stabilised 250v for first

anode of amplifier.
(c) was eliminated by removing some wiring ~~from~~ of the delay circuits to a point remote from the input grid.
Since making these mods there have been no corruptions.
I have been working on the "1"s being picked up by orders in the store programme My line was that spikes from tank decoding were letting thro digits but after much work in finding offending spikes I could not prove that they did correspond with the digits causing the corruptions
As an alternative method

[[NB05-061]]
of eliminating this possible cause Hemy produced the CT4+CT6 programme with modification for the transfer of the subsequent programme into different tanks ie avoiding spikes peculiar to one decoding.
Three programmes each modified differently all cause corruptions.
By producing new programmes which avoid operation of negative numbers, essentially the same programme works correctly.

20-2-51

A great day today - ~~The~~ One of the faults that has been dogging us for so long has been thrown out in the shape of a decoder. With this eliminated the "Royal" programme works correctly also the store test is done correctly with no faults.
The long general test fails however and we now are doing it piecemeal. G and E are OK but curiously enough A throws up a fault This is the dropping of the two most significant digits of of a negative number in the store

[[NB05-062]]
Of course the machine performs perfectly with a simple manual programme doing the same sort of job so that it looks like another of these difficult ones. We have also made half hearted attempts on another programme of Hemys which should do conversion of decimals to [[Tons Cwts qrs]] Lsd etc which may be useful as a demonstration JP is agitating for a table of squares programme which I feel may be quite within the scope of the m/c as it stands.

21-2-51

More progress to report.
The new demonstration program (conversion of various numbers to Lsd & t.L.qr lbs) has been made to work reliably. This has been achieved by a "frig" in the programme to avoid the subtraction of negative numbers on which the machine fails. Much time was spent with Hemy & Caminer trying various of their programmes and the result is that we know more or less what we can do. I have this afternoon been investigating the failures of the EDSAC Add

[[NB05-063]]
test and it appears to be due to cumulative affects of inefficient zero restoration. When a negative number is added into the accumulator the input has the contour

[[PULSE DIAGRAM]]

This can be traced back to the MSU but some is picked up on the way. The real cause of the trouble I feel is the exceedingly small input to the Acc IO (7 to 9 volts) where first amplification is made. These pulses are obviously not being amplified sufficiently

so that the clocking gate does not produce the required levelling off. Suggest a new amplified possibly after the MSU.

An amplifier in this position brings other problems with it. Introducing any extra delay in micand I line makes it necessary to do the same with mier (for collate) and AD2 together with adjustments in the delays in Acc IO & Complementor
Possible places would be
(a) after Mier I & AD 2 are mixed in collater

[[NB05-064]]
(b) Mier input to collater
<u>But</u> this would mean unclocked pulses passing around the machine and also Mier II is delayed and gated in collater to be mixed with a slightly delayed and ungated pulse in the complementer This also applies to Mier II being ~~amplified~~ mixed with Mier I and collated output in Collater.
Try amplifier at output of collater 33^{12} and 33^{14}
If this does not satisfy then problem calls for complete reconsideration of Acc input

system.
the Major gate pulse generator is now being used for synch to Raster Scope. It has already proved its worth again and again. However a change in logical design is called for in order that a D35 major cycle pulse can be used. Thus instead of producing a D0 directly [[in]] D35 sbe produced and thus delayed and amplified in [[counter carry]]

[[DIAGRAM]]

[[NB05-065]]

<u>Collater</u>

[[DIAGRAM]]

[[DIAGRAM]]

[[NB05-066]]
~~Pickup~~
~~Toys for Kiddies~~
~~Canvas 2 yds x 21" + 4 yds x 6"~~
~~Kite String~~
~~Fishing Tackle~~
Wood for
3/8 mild steel Rod. 2x 6ft 3x 3ft.
Bucket Seats for Car
~~baps~~
Butter Dish
Easter Eggs
~~Small Loud speaker~~
~~Towels~~

[[DIAGRAM - Sun lounger?]]

[[NB05-067]]
Stair Carpet 21 ft. 18"
Max Normal 2'6

[[DIAGRAM - dimensions]]

2'9

6'3 3'3 2'9

3'

Review of Position as at 26-2-51
Machine performs correctly following test Routines
A, S, I, O, G, E, L, X, Y, T, U,
Fault in logical design of collate prevents H, C
Fault in AD3 flip flop prevents R
Which leaves V only as a process which shows up an unknown fault.
Multiplication of sort can however be carried out as demonstrated by the fact that Initial orders are performed correctly
So that the immediate progems in producing a working m/c are

[[NB05-68]]
(a) Solve V fault.
(b) Solve Collate sign digit problem
(c) Solve Right Shift AD fault.

Having ~~achieved these~~ successfully passed this stage there are a number of other things to be done.
~~Draw up a f~~
As soon as the new CCUI with its full size alternate digits is available Marginal tests

are to be carried out in the computer. These should be followed by a general marginal test throughout the other units of the machine

The type of tests to be carried out must necessarily be the result of a good deal of thought and for that reason care must be taken to record results and the action taken to improve any likely faults shown up.
In parallel with this work there are jobs to be done throughout the machine.
(a) Modifications as listed elsewhere
(b) Valve numbering
(c) Pulse wiring
(d) New Battery to be filled
(e) Control Desk to be filled up.
(f) Wiring of temporary controls

[[NB05-69]]
to be passed over to the control desk

V tests
Machine interpretting A_{24D} incorrectly

26-2-51

Feedback in Waveform Circuits

F J U ~~Whit~~ Ritson
Uses of feedback
- Paraphase
- Cathode Followers
- Reducing No of Parameters in cct
- Impedance Conversion

Cathode Follower
- Simplest & widely used as impedance conversion.
- Properties
  - V of amplif $E_0/E_2 < 1$
  - Output Impedance small
  - Input Impedance large

"error actuated" device

e_2 = 50v	R = 10K	e_0 = 54	e_g = -4
e_2 = 100	R = 10K	e_0 = 102	e_g = -2
Diff B_2 50		58	

[[NB05-070]]
what effects of gm & R_K.
very small for reasonable changes

[[PULSE DIAGRAM]]

t = 1/gm C

Cathode follower with capacitive load.

[[PULSE DIAGRAM]] R_KC

If CF returns to negative potential sharper returns

[[PULSE DIAGRAM]]

Input impedance

[[DIAGRAM]]

effect almost nil due to low voltage across it

See Saw

[[DIAGRAM - CIRCUIT]]

Gain R_2/R_1

[[NB05-071]]

[[DIAGRAM - CIRCUIT]]
[[DIAGRAM - CIRCUIT]]

$i = e_g(1+m) / R_2$

$e_g/i = R_2 / 1+m$

if m .i [[$\propto$]] then input impedence is virtual earth

any current fed in flowout thro R_2

$i_1 = R_1 / R_2$
[[DIAGRAM - CIRCUIT]]

$e_2 = R_2 / R_1 \, e_1$

If m is order of 100

equiv circuit
[[DIAGRAM - CIRCUIT]]

$e_q = R_2/1+m \, e_1 / R_1 + R_2/1+m$ $\qquad$ $e_0 = me_g$

$e_0 = m / 1+m \, . \, R_2 / R_1 + R_2/1+m \, e_1$

Voltage amplification $e_0/e_1 = m/1+m \, . \, R_2 / R_1 + R_2/1+m$

[[NB05-072]]
$\therefore$ when m >> 1
$e_2/e_1 = R_2 / R_1 + R_2/1+m$

10^6
$10^6 + 10^6/1+10^3$
1001 . | 1000~~000~~
9009
9910
9000

further increase of m
$e_2/e_1 = R_2/R_1$

example
(1) m = 1000 (three stage)
$R_1 = R_2 = 1\ M\Omega$
$e_0/e_i = 0.998$

(2) m = 100 $R_1 = R_2 = 1$ Meg
$e_0/e_i = 0.98$

(3) m = 10 (triode)
$R_1 = R_2 = 1\ M\Omega$
$e_0/e_i = 0.833$

Output Impedance

make input zero & set screen so that output is zero, connect battery to output [[ten]] to δe_0

$i = \delta e_0 / R_1 + R_2 + \delta e_0 / R_a + g_m R_1 / R_1 + R_2 . e_0$

∴ output impedance (resistance)

$= \delta e_0 / i = 1 / 1/R + 1/R_1 + R_2 + R_1 / R_1 + R_2 g_m$

when $R_1 = R_2 = 1$ meg $R = 50$ K
$\approx 2 / g_m$

[[NB05-073]]
See saw as an adder

[[DIAGRAM - CIRCUIT]]

Generalising

[[DIAGRAM - CIRCUIT]]

$m = e_0 / e_1$

impedence between a & b

$= Z / 1 + m$

provided does not oscillate

equivalent circuits

[[DIAGRAM - CIRCUIT]]

From this derive Miller Integrator

[[DIAGRAM - CIRCUIT]]

equiv [[cct]]

[[DIAGRAM - PULSE]]

$\Delta e_2 = - E_1/CR$

[[NB05-074]]
accuracy of integrations

let m = 100 [[DIAGRAM - CIRCUIT]]
C = 1μF
R = 1MΩ
E_1 = 100v
initial current $i = E_1 / R$
but $i = E_1 - e_g / R$

by making m large apparent capacity e_2 starts at HT
~~Input~~ . i = 100 / 1MΩ = 100 μA
$di_2/dt = i/c = 100/10^6 x100$ t = 100v S.

After anode has rundown 250v
∴ grid rises ~~25v~~ 250/.m = 2.5 volts
voltage across R = 97.5
$i = 97.5 / 10^6 = 97.5$
rate of rundown = 97.5 vS.

26-2-51

Machine was out of order this morning on starting up. Found to be due to Mier Tank again. After putting this right Test Tapes were put on showing up faults in S (5 in 1000) Store (Tank No 5 out of order.) Others OK. C, H, V, R not tried.
Later I found that Hemy had provided revised tapes for H & C not using collation of negative numbers. These worked O.K. The Demonstration progamme of Sterling & Weights conversion performed correctly for JRMS after a mishap with the tape at the start

[[NB05-075]]
Hemy has produced three versions of the store decoding check but so far~~e~~ none work properly.
I have been concentrating on V and so far~~e~~ have found that the simple multiplication of -1 x 1 goes wrong. This seems to be due to an extra digit or digits being added in as if done on single shot the result -1 appears for a split second but then disappears leaving a single 1 in the less significant half of the accumulator

The fact that the machine is virtually working brings the question of a full scale demonstration well into the picture. It is visualised that the sterling & weight conversion programme will be used together with a possibility of a small wages programme The wages programme has not been tried on the machine as yet mainly because it was felt that with so many things not quite correct it would be asking too much. Now that V & R are the only functions that are not answering correctly to the

test programmes it is quite likely that these programmes

[[NB05-076]]
might be performed correctly
A new gadget which would prove of use and which I must get made is a visor to split up the Raster Scope picture into component parts. ie.

Action	Tank	Time	L/S
5	6	5	1

~~BI~~
[[DIAGRAM]]

[[DIAGRAM - HORIZONAL]]

Action Tank Time L/S L/S

TANK	COMMENCING AT
1	32
2	64
3	96
4	128
5	160
6	192
7	224
8	256
9	288
10	320
11	352
12	384
13	416
14	448
15	480
16	512
17	544
18	576
19	608
20	640

[[NB05-077]]
(a) Piece of thin [[paxoline]] sheet.
(b) Cut rectangular Hole size of Raster
(c) Holes for thread.
(d) Labels for [[graticule]]

Action	Tank No	Compartment	L/S
			0
			2
			4
			6
			8

10
12
14
16
18
20
22
24
26
28
30

31

Conversion table for tank No (X32)
from 1 to 64 in 4 parts to be pasted to Scope chassis

27-

Fundamentals of Programming
T.R.T.
Location - in which compartment number or order is stored

Tape	Action
	Address
S-----	Suffix

Action
(A) 28 Add.
(T) 5 Transfer
(U) 7 Copy
(S) 12 Subtract
(H) 21 Set Up Mier
(V) 31 Multiply
(L) 25 Left Shift
(R) ~~8~~ 4 Right Shift

[[NB05-078]]

[[DIAGRAM]]

S x S to S -> L16 to L -> R2
S x L to S -> L34
L x L to L -> L34

Left Shift Suffix 17 = 0
19 = 1

1 place 25 - 19

2	"	25	1	17
3	"	25	2	17
4	"	25	4	17
5	"	25	[[2^{r-2}]]	17

Action

27	G.	Negative Test
3	E	Positive Test

27-2-51

Yet more progress. LEO has now done the V test programme sucessfully without a fault. Occasional faults on the S test still crop up but as they are not more than two or three in a thousand it will be difficult to trace. I hope these will resolve themselves into something more get-at-able when attenuator tests are done later

[[NB05-079]]
The solution to the V problem was to put the amplification of the digits going to the acc after the MSU instead of after the collater. This in. itself did not clear the trouble completely and an adjustment had to be made to the gain in the Complementer (not unreasonably) This leaves only the R programme outstanding.
A second fault which has defied the test programme reared its ugly head again today - a D_{27} corruption in tank 2 when being put into tank 6.

This was found to be due to a spike being applied to the input gate of Tank 2 The origin of the spike is a bit of a mystery as it occurs only during the coincidence waveform and my previous explanation of it being due to differentiation of the Tank No SR waveform set by D_{27} (F_9) is therefore void.

[[NB05-080]]

28-2-51

The spikes have been explained to some extent. They are due to the set pulses received by SRs during the time that they are set. They do not appear on the + waveform but spikes of the order of 10-12 volts appear on the - waveform. The mystery of how these spikes persist through the double wiping action of two decoders is not so clear.
[[An unusual]] programme was used today to investigate these spikes and it was found that they were present not only for D_{27} but also for D_{25} & $_{26}$

Now D_{25} & $_{26}$ are used for the Rack Decoding so that in these cases the waveforms have been thro two decoders and have therefore been "wiped" twice.
It is not easy to remove these spikes by [[wiping]] still further as the waveforms are only 20 volts at the Storage Units and if made smaller they would be rather marginal for use as clear waveforms
An easier way to remove the spikes completely would be to allow only one

[[NB05-081]]
set pulse. This could be achieved fairly easily by gating the OT or SCT pulses with W_{15} in Panel 12
this occurs for one or a half of a minorcycle at the begining of stage I & stage II

[[DIAGRAM]]

I am still awaiting CCU I before I can get on with marginal tests and I am assuming that the occasional Z's which are

thrown up by EDSAC Tests will be eliminated when these have been satisfactorily carried out.
I must work out a schedule of operations before embarking on these and no one fault can be corrected without reference to all other tests involving the unit calling for modification.
~~Probably the best procedure will be first of all to put the Test programmes in some sort of order and then working on the first of~~

[[NB05-082]]
~~these~~
~~(a) insert max attentuation in all leads in turn affecting the function being tested.~~
~~(b) Where one of~~
First of all design short manual programmes for each function to be tested and
(a) insert max attenuation in all leads in turn affecting the function
(b) Where a fault is thrown up establish the exact nature and cause but do not modify permanently

~~Attentuator Tests~~

1-3-51

Very little progressive work on the machine ~~this~~ today. After a discussion on immediate tasks, most of the time was spent in trying out programmes for Hemy & Caminer
One fault that cropped up today was a faulty valve with no emission in one half which just died suddenly in the ACC SU I. It took about 3 minutes to find & replace.
A second fault that has been with us intermittently for some days and which

[[NB05-083]]
appears to be getting worse in that occasionally some of the initial orders fail to get into the store. It appears to be due to more than one cause as sometimes the SCT is not stepped on at the same time.
Occasionally it is just the first EP which is lost ~~but~~ and this results in all the orders being misplaced by one position. But less often it may be several positions or even all of the starter orders all piled on top of each other in the

first position of the store.
It is a fault which does not happen sufficiently reliably to give the necessary information for reliable diagnosis.
A similar effect was occurring much more frequently this afternoon but after replacing a grid leak in the input to coincidence unit of the OT / SCT number, the effect was almost completely removed. The theory here was that the grid was floating due either to O/C megohm or dry joint as the application of the

[[NB05-084]]
finger on the grid of the valve cured the effect.

Preparation for
attentuator checks on arithmetic [[unit]]

(a) Accumulator loop. (inc RL)
(b) E 3
(c) G 17
(d) A 28
(e) S 12 T 5
25 < U 7
(f) L control
(g) R control
(h) H 21
(i) C 30
(j) V 31
1
0
(k) X 26
(l) Y 6

every good [[illegible acsounliun?]] seems to underst learn, remember Hard calculus variation in order X Y Z

[[NB05-085]]
Sewing Machine Motor
Use 5000Ω in series with com (?)
Approximate power consumption 180 watts (compared with 60 watt lamp. Shorting out 5000Ω increases consumption by 25% and causes sharp breaking action.
Speed control can be achieved by stop-start foot switch, slow acceleration making smooth control possible.

R Amplifier
Car Seats
Simmons [[Fram]]
Burton [[Radio]]
[[Foam]]
Decoke .
Small Room

[[NB05-086]]

Pulse Operated Time Bases
Dr H.A.Dell

$C = [[U]] / V = \int i\, dt$

$dV/dt = 1/C\ i$

[[DIAGRAM - CIRCUIT]]

[[DIAGRAM - CIRCUIT]]

Sq wave

Elimination of initial drop

[[NB05-087]]

[[DIAGRAM - CIRCUIT]]

miller circuit without initial drop.

-6 to +5

Sanatron (produces own sq wave

[[DIAGRAM - CIRCUIT]]

R_1C_1 is made almost the same as RC so that the rundown is differentiated into a square wave
no waiting after anode bottoms
trigger pulses during rundown are ignored.
[[brighting]] waveform available at anode of second

[[NB05-088]]

[[DIAGRAM - CIRCUIT]]
[[Catch]] of anode to ~~preven~~ obviate valve variations
[[1250]] cleans off suppressor chars variations

By using above diodes on a variable potentiometer a variable delay

Bootstrap

[[DIAGRAM - CIRCUIT]]

$C_1 >> C_2$ sawtooths Positive going

[[NB05-089]]

5-3-51

Very interesting lecture this evening on timebases. Dr Bell took us thro the RC condenser charging circuit, the constant current device and then on to Miller in various forms finishing up with the [[sanatron]]. I think that at least for a few hours I have the working of the sanatron clear in my mind.

Machine was out of action today. It was not until fairly late this afternoon that I had the units that had been modified since Friday, in place ~~and Then the~~ First the starter seems to be giving trouble as the first [[S]]P (mechanical) does not step on the SCT so that the first two orders go into position 0. If W13 is left in the set condition however this works out OK but the initial orders fail to take in the tape. I have not investigated further but it would seem that there is

[[NB05-090]]
a comparatively simple explanation for this.

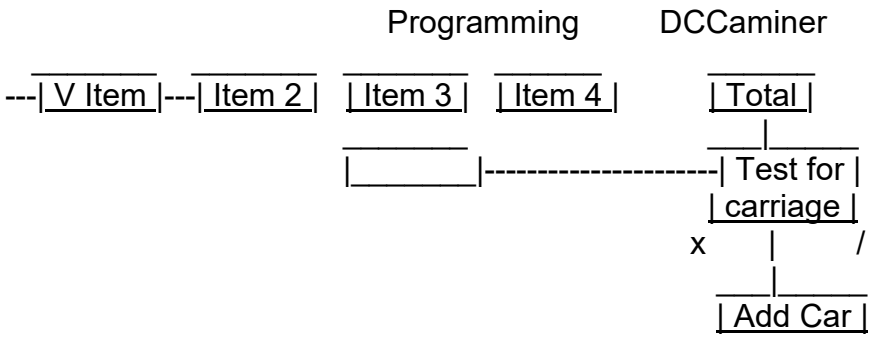
On Wednesday there is to be an enforced shut down when Mr Williams staff will install new HT supply. During that time there will be further mods to [[units]] of the machine so that least possible time will be lost in bringing it to completion Tomorrow I have to get it working as before so that after the latest mods have been put in there will not be any multiple faults to

contend with.
Units to be "modified" are
(a) Output unit (8)
(b) Collate
(c) Coord initial reset and Z order
(b) General Rack Wiring.

Thin glass tube iron ~~filings~~ powder
magnetic force set up
electrostatic reading

[[NB05-091]]

6-3-51



+ From Pay 64
- I Tax 65
- Personal 66
- N Ins. ---------- Code is 63

+ Net Pay 67

Code 1 91
" 92
" 93
" 94
" 95
" 96
Code 7 97

Store common order 12/90/17

7-3-51

Today commences the enforced shut down while new HT supply is fitted. This should ~~last~~ be completed by Monday so that we have 3 days for mods.
It was a race against time yesterday to get the machine working after the last mods

were made. These were on Coord (removing of spikes) and MSU (amplifiers). So as to complicate the issue two other faults had to crop up at the same time

[[NB05-092]]
so that in addition to getting the two new units into operation I had to deal with an intermittent short on one of the W13 flip flop valves, and ~~an~~ a diode in the Coord IV
The state of affairs at 6.45 last night however was that all test programmes with exception of R & V give a perfect response. I had no time to investigate V further but as it appeared to be one of the factors in one of the multiplication that was wrong rather than the multiplication

itself I felt justified in leaving it.
Work for today is first of all to get various people started off on their different jobs. The girls will clear up valve numbering. Gibbs will do various items of rewiring on the racks and also clean up the starter unit. Dutton is due for a big mod on the Output Units, & Shaw [[a small]] rewiring of the collater to cover negative numbers.
I have to get all these jobs clear in my own mind before starting anyone off

[[NB05-093]]
so that I have some quick thinking to do first:
Gibbs can start on the starter without any special instructions.
~~D~~ I have already got a circuit for Dutton to work [[a]] on the Output Units
Shaw can get some units out for the girls to number while I decide on the Collater Mods
I must then decide on the next wiring changes necessary so that Gibbs can proceed on this as soon as the starter is finished

When I have every one [[happy]] other work I can give my attention to the Right shift flip flop which so far refuses to stay up longer than 8 minorcycles. Whether it will be possible for all the work necessary to proceed without [[interacting]] is doubtful but an attempt will be made.

[[NB05-094]]
The [[Gallery]] Proofs of my article arrived from EE yesterday and must be returned today. I see that they have omitted the appreciation which I asked for. I think it was something like
The author would like to express his appreciation of the work done by Mr R T Shaw in building and testing the instrument described in this article

[[UPSIDE DOWN]]
Collate Negative No Sign.
~~gate OT & SCT. with W15~~
Clear store

[[NB05-095]]
[[BLANK PAGE]]

Outstanding Modification
1. Z order & resetting of W13 in bogus stage II (S)(1)
2. Operating Control stepping control and mech EP.

~~3. Tape Reader~~
4. AD flip flop for right shift (S)(4)
5. Termination in Storage Junction
~~6. F_1 - diode in Transfer Unit~~
~~7. " " " Coincidence "~~
~~8. " " " ACC IO~~
9. CCU I (2)
10. Initial resetting of DC flip flops
11. Clear Acc Waveform to 1 m/c
12. Output Unit operation of relays (3)
~~13. Amplifiers in Add line.~~