GEC COMPUTERS LIMITED

USER HARDWARE HANDBOOK
– SYSTEM ENGINEERING
(PROCESSOR PERFORMANCE)

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PROCESSOR PERFORMANCE

CONTENTS

TABLES

1 INTRODUCTION

Four of the five sections in this manual each describes one aspect of the performance of the 4080:-

(a) Section 2, the Central Processor Unit (CPU) instruction times

(b) Section 3, the Basic Multiplexor Channel (BMC) transfer times

(c) Section 4, the effect of an intermediate link and its cable on the BMC transfer times

(d) Section 5, a summary of peripheral controller signal turn round times.

Each section, except (d), gives a brief description of the relevant parameters and the methods used in assessing them together with tables giving the times taken to perform each of the listed functions.

Section 5 consists of a list of peripheral controllers with a table showing their contribution to the channel controller's instruction times.

All the parameters given (unless otherwise specified) have a $\pm$ 10% tolerance which applies over the specified operating range of the equipment. The calculated parameters are based on a CPU clock time of 250 ns and a store cycle time of 550 ns.

The various parameters only apply if the CPU or BMC, as appropriate, has sole use of the store interface. In practise the CPU and BMC share the store interface and, consequently, the performance of both is reduced slightly. The effect varies from time to time depending on the CPU instruction mix and the type of BMC operation. To allow for this factor an overall allowance of 10% may be added to any times calculated from these parameters (e.g. program runtimes). Critical cases should be referred to GEC Computers Ltd.

1.1 INPUT-OUTPUT PERFORMANCE

To use this manual the following procedure should be followed assuming that it is required to find the channel controller performance for a particular peripheral controller:-

(1) Take the peripheral controller turnround times from section 5. If the controller is not listed (e.g. a user's own device) the turn round times should be calculated using worst case figures.

(2) Knowing which channel controller is concerned use the turn round times to obtain the various waiting times from the table in section 3 remembering that if the channel to peripheral controller connection is via an intermediate link the waiting times are modified as detailed in section 4.

(3) Use the waiting times in the formulae in either section 3 or section 4 as appropriate to obtain the various transfer times on the Normal Interface for a particular peripheral connected to the BMC.

The detailed Normal Interface performance data for the standard GEC peripheral controllers is given in the Systems Manual.

2 CPU INSTRUCTION TIMES

This section is divided into three sub-sections. The first specifies the instruction times of the ordinary arithmetic and logic operations. The second specifies the basic nucleus operation times, and the third specifies the nucleus operation times.

2.1 ARITHMETICAL AND LOGICAL INSTRUCTIONS TIMES

This subsection deals with both integer and floating point mode instructions. An additional time must be added to the tabled times for the additional operand fetch and subsequent processing involved in formats A3, A4, and A5. The times are:-

Formats A3, A4	1.05/us
Format A5	0.75/us

The tabled instruction times are valid for formats A1 and A2.

Format A Integer Mode, Arithmetical and Logical

Instruction	Time (/us)	Instruction	Time (/us)	Instruction	Time(/us)
AD	1.10	INCS	1.85	NX	1.10
ADW	1.65	LBX	1.10	OBS	1.90
ADX	1.10	LD	1.10	SB	1.10
ADY	1.35	LDB	1.10	SBW	1.65
ADZ	1.35	LDM	5.95	SBX	1.10
CP	1.10	LDW	1.65	SBY	1.35
CPB	1.10	LDX	1.10	SBZ	1.35
CPW	1.65	LDY	1.35	ST	1.35
CPX	1.10	LDZ	1.35	STB	1.35
D	20.35	M	5.85	STM	5.45
DECS	1.85	MW	10.40	STW	1.90
DW	20.40	MX	3.60	STX	1.35
DX	6.60	N	1.10	STY	1.35
HAY	1.05	NBS	1.90	STZ	1.35
HAZ	1.05	NW	1.65	XBS	1.90

Format L Integer Mode, Arithmetic

Instruction	Time (μs)	Instruction	Time (μs)
ADL	1.05	LDXL	1.05
ADXL	1.05	LDYL	1.05
ADYL	1.05	LDZL	1.05
ADZL	1.05	ML	5.80
CPL	1.05	MXL	3.55
CPXL	1.05	NL	1.05
CPYL	1.05	NYL	1.05
CPZL	1.05	SBL	1.05
DL	20.30	SBXL	1.05
DXL	6.55	SBYL	1.05
LDL	1.05	SBZL	1.05

String Instructions

In the following table the factor N refers to the number of bytes (or halfwords in the case of the MHS instruction) to be moved.

Instruction	Time (μs)
CPBS	1.55 + 3.1N
MBS	1.55 + 2.35N
MHS	1.55 + 2.35N
SCBS	1.55 + 3.6N
TRBS	1.55 + 3.4N

Shift Instructions

In the following table the factor N is defined as $\frac{n}{4}$ + the remainder, where n is the number of places shifted.

For example:-

if n = 11 then N = 5 (2 + 3)
if n = 12 then N = 3 (3 + 0)
if n = 13 then N = 4 (3 + 1)

Instruction	Time (μs)
SBAL	2.30 + 0.5N
SBAR	2.30 + 0.5N
SL	1.80 + 0.25N
SLC	1.80 + 0.25N
SR	1.80 + 0.25N
SRL	1.80 + 0.25N
SXL	1.80 + 0.25N
SXR	1.80 + 0.25N

NOTE: For indexed instructions add 0.25 μs to the above figures.

Bit Instructions

Instruction	Time (μs)
CLRB	1.30
CLRBX	1.55
LDBT	1.55
LDBTX	1.80
SETB	1.55
SETBX	1.80
TGLB	1.55
TGLBX	1.80
TSTB	1.55
TSTBX	1.80

Miscellaneous Format L Instructions

Instruction	Time (μs)
PEC	1.55
RK	1.30
SEXT	2.05

Format A, B and L Branches

Instruction	Time (μs)	
	Branch Taken	Not Taken
B	1.35	1.35
BI	2.40	2.40
BL	1.35	1.35
BLI	2.40	2.40
BN	1.35	1.10
BNCA	1.35	1.10
BNN	1.35	1.10
BNP	1.35	1.10
BNZ	1.35	1.10
BOF	1.35	1.10
BP	1.35	1.10
BPAR	2.35	1.30
BZ	1.35	1.10

Format RR

In the tables that follow the instructions are divided into two groups RNA and OTHER. This latter expression covers:-

RAD, RADC, RADI, RCP, RI, RLD, RN, RO, RSB, RSBC, RSBI, RX.

The instruction RNA is in a group by itself.

Format RR Branches

A format RR branch is any instruction in which the destination register is the S register.

Instruction	Source	Destination	Time (μs)
OTHER	A or B	S	2.60
OTHER	$\overline{\text{A or B}}$	S	2.35
RNA	Any	S	2.10

Other Format RR Instructions

Instruction	Source	Destination	Time (μs)
OTHER	A or B	$\overline{\text{S}}$	1.55
OTHER	$\overline{\text{A or B}}$	$\overline{\text{S}}$	1.30
RNA	Any	A or B	2.05
RNA	Any	$\overline{\text{A or B or S}}$	1.55

Floating Point Instructions

In the tables that follow the times marked with an asterisk are average times, based on a statistical analysis of the operators and operands used in a typical situation.

Format A

Instruction	Time (μs)	Instruction	Time (μs)
EAD	7.66 *	FCP	2.58 *
ECP	3.28 *	FD	19.40
ED	60.25	FIX	13.40 *
ELD	3.75	FLD	2.15
EM	35.00	FLT	5.90 *
ESB	7.66 *	FM	10.90
EST	3.75	FSB	5.80
FAD	5.80 *	FST	2.15

Format L

Instruction	Time (μs)
FNEG (normalised)	1.80
FNEG (not normalised)	2.55
SFM	1.80
SIM	1.80

2.2 BASIC NUCLEUS INSTRUCTION TIMES

The basic nucleus instructions consist of input/output and interrupt related instructions.

In the following table, T is the Channel Controller time for a program output (e.g. approximately 6.4μs for a teleprinter on the basic multiplexer channel).

Instruction	Time (μs)
AINT	3.85
IN	3.75 + T
INH	1.80
OUT	3.75 + T
PERM	1.80
SINT	9.80
TERM	7.35

The time taken to handle an interrupt, that is the time between concluding the current instruction and starting the instruction to which the machine has been directed by the interrupt, is 9.80μs.

2.3 FULL NUCLEUS INSTRUCTION TIMES

Definitions

In this section the following terms are used:-

(a) A route is said to be closed if a message sent on that route does not change the state of the destination process. A route is said to be open if a message sent on that route results in a change of state of the destination process. Thus a route is open if:-

(i) the destination process is in the free state,

(ii) the destination process is in the wait state for this route.

(b) A process is said to have a Message Pending if:-

(i) it is in the free state and at least one message is waiting to be processed,

(ii) it is in the wait state and there is a message on the awaited route.

(c) A semaphore is said to be free if it is not claimed. A semaphore is said to be held if a process has claimed it but no further process has attempted to claim it. A semaphore is said to be complex held if it is claimed and at least one further process has attempted to claim it.

(d) Ts - time taken for schedule operation

	Time (μs)
Time to access scan N words where N is in the range 0-15	2.95+1.3N
Time to examine each bit of scan word that is set(i.e. selectable)	2.05
For process in wait and pass priority state,extra time for each process in priority chain.	1.30

(e) Tn - time taken to load up a new process or restart an existing process

	Time (μs)
No process change No messages to be picked up	3.70
Fixed message to be picked up	11.25
Queued message to be picked up	16.05
Process change No message to be picked up	23.05
Fixed message to be picked up	26.30
Queued message to be picked up	31.10

Full Nucleus Instructions

(a) *Semaphore Instruction*

(i) Claim

	Time (μs)
Semaphore Free (No Process Change)	4.40
Semaphore Held (Process Change)	4.65+Ts+Tn

(ii) Release

	Time (μs)
No attempted claims	4.15
Further attempted claims	6.25+1.85N +Ts+Tn

where N = number of processes claiming the semaphore

(iii) Conditional Claim

	Time (μs)
Successful	4.40
Unsuccessful	4.15

(b) *Segment Instruction*

	Time (μs)
Store CST	4.0
Load CST 3	7.95
Load CST 0, 1 or 2	7.40
Conditional Load CST 3	8.70
Conditional Load CST 0, 1 or 2	8.15

(c) *Interchapter Branch*

	Time (μs)
ICB - no segment change	4.60
segment change	9.10
ICBL - no segment change	6.25
segment change	10.75

(d) *Input/Output*

	Time (μs)
Program Cycle	8.45+T
Start Autonomous cycle & load WCB	12.05+T+T_1

where T = Channel Controller time for program output cycle. Section 4 gives a method of calculating this - for a teleprinter it is 6.4μs.

T_1 = response time of channel - this depends on what operation (if any) the channel is engaged on, for the BMC this is at least 250ns.

(e) *Interrupt*

The times quoted below are calculated from the point at which the CPU picks up the interrupt i.e. at the end of the scheduler, beginning of scheduler or end of instruction.

	Time (μs)
Closed route	8.70
Open route higher priority	24.8+Ts+Tr
Open route lower priority	10.1+Ts

where Tr = time for the channel to respond to a CPU request to read status and count from the WCB. This has a minimum of 250ns for the BMC if it is idle. Its maximum value is that of the highest 'burst time' for any peripheral on the system.

(f) *Interprocess Message and State Change Instructions*

The times quoted below are for sending messages via fixed buffers. To send a message via a queued buffer requires an additional 5.5μs

(i) No message - Go Free

	Time (μs)
Message pending fixed route	17.9
queued route	23.25
No message pending	8.6+Ts+Tn

(ii) No Message - Wait for Reply

	Time (μs)
Correct message pending	
fixed route	17.9
queued route	20.4+1.6N
Incorrect message pending	
fixed route	9.4+Ts+Tn
queued route (none in queue)	10.4+Ts+Tn
queued route (none in queue)	11.15+1.6N

(iii) Send Message - Continue Running

	Time (μs)
Closed route	13.0
Open route higher priority	13.9+Ts+Tn
lower priority	17.6+Ts

(iv) Send Message - Go Free

	Time (μs)
Closed route fixed message pending	25.45
queued message pending	30.25
no message pending	15.75+Ts+Tn
Open route message pending	17.15 + Ts + Tn
no message pending	18.25 + Ts + Tn

(v) Send Message - Wait for Reply

The times are as stated in (ii) above with the following additions:-

closed route - additional time required to set destination state and load buffer 9.4 μs

open route - additional time required to load buffer, schedule, and load new process if necessary 9.4+Ts+Tn μs

3 BMC TRANSFER TIMES

This section generates formula which enable the BMC transfer times to be calculated using information in Sections 4 and 5 as necessary. The formula for each of the transfer times has two parts; the first a fixed time calculated from the number of microsteps and store cycles required, and the second a time which depends on such factors as 'cable' delays and the turn round times of the particular peripheral controller being considered.

The term 'cable' delay includes the transmission delay along backplane(s) and through any inter-unit link cards as well as pure cable delays. This is dealt with in section 4.

Section 5 lists the peripheral controller signal turn round times.

3.1 THE WAITING TIMES

In the following, parameters are used as defined below:-

(a) Px is the 'cable' delay incurred by signal x

(b) TPxy is the peripheral controller turn round time involved in receiving signal x and responding with signal y.

(c) TCxy is the channel controller turn round time for signals xy

(d) Px + TPxy + Py is a component of the waiting time depending on the particular peripheral controller and the manner in which it is connected to the BMC.
As this section is concerned only with controllers mounted in the same unit as the BMC the 'cable' delays Px and Py are negligible. However Px and Py are retained in the formulae generated to make the formulae applicable when they are not negligible.

Turn Round Times

The following peripheral controller signal turn round times are specified (refer to the Normal Interface section of the Interfaces Manual for a definition of the signals named):-

(a) TP_{12} is OUTTIME going true to ENGAGED set true

(b) TP_{34} is PROCEED going true to INTIME set time

(c) TP_{56} is OUTTIME going false to INTIME set false

(d) TP_{74} is OUTTIME going false to INTIME set true

(e) TP_{57} is INTIME going false to OUTTIME set true; this, as measured at the channel controller, is 240ns for the BMC with the variable delay set to 100ns.

Table of Waiting Times

The BMC logic is essentially synchronous so the Waiting Times are an integral number of the 250ns clock periods. The tables can be used by knowing the peripheral controller turn round times and reading off the waiting time. The turn round times for GEC standard peripherals are listed in section 5. A User connecting his own peripheral controller must calculate these parameters for his own equipment.

(a) *W1 - OUTTIME True to ENGAGED True*

(P_1 + TP_{12} + P_2) ns	W1 µs
0 to 129	0.50
130 to 379	0.75
380 to 629	1.00
630 to 879	1.25
etc.	etc.

(b) *W2 - PROCEED True to INTIME True*

(P_3 + TP_{34} + P_4) ns	W2 µs
0 to 249	0.50
250 to 499	0.75
500 to 749	1.00
etc.	etc.

(c) *W3i- (Input) - OUTTIME False to INTIME False*

(P_5+ TP_{56} + P_6) ns	W3i µs
0 to 99	0.25
100 to 349	0.50
350 to 599	0.75
etc.	

(d) *W3o (Output) - OUTTIME False to INTIME False*

(P_5 + TP_{56} + P_6) ns	W3o µs
0 to 99	0.50
100 to 349	0.75
350 to 599	1.00
etc.	etc.

(e) *W4 - OUTTIME True to INTIME True - Burst Mode Output*

(P_7 + TP_{74} + P_4) ns	W4 µs
0 to 799	0
800 to 1049	0.25
1050 to 1299	0.50
etc.	etc.

(f) *W5 - OUTTIME True to INTIME True - Burst Mode Input*

(P_5 + TP_{56} + P_6 + TC_{57} + P_7 + TP_{74} + P_4) ns	W5 µs
0 to 89	0.50
90 to 339	0.75
340 to 589	1.00
etc.	etc.

Table 1: BMC WAITING TIMES

3.2 THE TRANSFER TIME FORMULAE

The BMC transfer times in microseconds, are specified in terms of a fixed time and the Waiting Times W1, W2, W3i, W3o, W4 and W5.

(a) Program Input Cycle

$$T = 4.40 + W1 + W2$$

(b) Program Output Cycle

$$T = 4.65 + W1 + W2 + W3o$$

(c) Status Break Cycle

$$T = 3.90 + W1 + W2$$

(d) Autonomous Transfer Cycle

(i) Output of a single byte or halfword

$$T = 4.95 + W1 + W2 + W3o$$

(ii) Additional output burst mode

$$T = 1.30 + W3o + W4$$

(iii) Input of a single byte or halfword

$$T = 4.95 + W1 + W2 + W3i$$

(iv) Additional input burst mode

$$T = 1.05 + W5$$

The above fixed times for autonomous transfer cycles take no account of the effect of concurrent CPU to store accesses. An approximate allowance for this effect may be made by increasing the total times by 10%.

4 THE EFFECT OF AN INTERMEDIATE LINK ON BMC PERFORMANCE

The intermediate link and its associated cables modify the performance of the Normal Interface in three ways:-

(a) a backplane delay is introduced

(b) cable delays are introduced

(c) delays occur as signals are processed on the intermediate link card

Two types of transfer cycles are considered, type (1) which includes program cycles, status break cycles, and single autonomous cycles and type (2) which consists of burst mode cycles.

This section takes the backplane transmission delay to be 10ns worst case and the intermediate link cable delay to be 28 ns (i.e. 14 ft at 2 ns per ft.).

4.1 TRANSFER CYCLES, TYPE (1)

The use of an intermediate link imposes the following worst case values for the 'cable' delay parameters Px specified in section 3.

P_1 = 269 ns - Program or Status Cycles
P_1 = 306 ns - Autonomous Cycles
P_2 = 207 ns
P_3 = 149 ns
P_4 = 209 ns
P_5 = 277 ns
P_6 = 159 ns
} All Cycles

4.2 TRANSFER CYCLES, TYPE (2)

Burst mode transfers through an intermediate link causes certain of the waiting times tabled in section 3 to be modified and made peripheral controller independent.

When the link recognises OUTTIME false from the channel it returns INTIME false to the channel with the result that the following waiting times take fixed values:-

W3 i	500 ns
W3o	750 ns
W4	$202 + (T_{56} + T_{74} - 26)$ * ns
W5	$202 + (T_{56} + T_{74} - 26)$ * ns

*Note that if $(T_{56} + T_{74} - 26)$ is negative it is ignored.

4.3 PRACTICAL EFFECT OF USING A LINK

The practical effect of an intermediate link is to increase the primary Normal Interface loading, for those peripherals connected to the link, by an average of approximately 10%.

If a second link is connected in series with the first the net effect is to increase the Normal Interface loading by about 20%. Consequently, if possible, intermediate links should fan out from the CPU rack and not be series connected.

5 SUMMARY OF PERIPHERAL PERFORMANCES

This section lists the normal interface signal turn round times for each of the peripheral controllers, using the parameters defined in section 3.

These times are dependent of type of channel controller.

Peripheral Controller	TP_{12}	TP_{34}	TP_{56}	TP_{74}
9 Track Magnetic Tape	429	428	438	62
Card Reader	1405	955	1411	–
Disc (Cartridge or HPT)	362	368	378	62
Paper Tape Reader (500)	1495	1235	1735	–
Paper Tape Punch (110)	1495	1235	1735	–
Lineprinter	925	673	895	491
Control Teleprinter	712	448	553	–
Async Comms Controller	621	448	548	–
Sync Comms Controller	576	416	548	–
Multichannel Comms. Cont.				
(Input)	465	1309	1328	–
(Output)	465	465	1328	–

Those peripherals for which TP_{74} is not defined do not operate in burst mode.

These peripheral turn round times are absolute worst case and are given in nanoseconds.

Table 2: PERIPHERAL TURN ROUND TIMES