

GEC COMPUTERS LIMITED

**USER HARDWARE HANDBOOK
— SYSTEM ENGINEERING
(SYSTEM DESCRIPTION)**

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Supplement 2:	Ready Number Allocation

1 INTRODUCTION TO HARDWARE USER HANDBOOK - SYSTEM ENGINEERING

The System Engineering Handbook is structured to provide a system engineer with basic information necessary to gain an overall appreciation of the GEC 4080 computer system. This basic information is expanded to include all the information required to plan, and arrange for, the installation of a complete configuration (system) or any of its units.

The Handbook comprises the following manuals, each of which covers a distinct aspect of the subject.

System Description Manual (This manual.)

Installation and Standards Manual

Interfaces Manual

Processor Performance Manual

4080 CONFIGURATION - INTRODUCTION

2.1 CONFIGURATION

A GEC 4080 configuration consists of standard units supplied by GEC Computers Ltd., supplemented as necessary by other GEC products (e.g. March 4 process peripherals), or by user supplied equipment. The standard GEC units are listed and briefly described in Supplement 1.

The GEC 4080 and its associated equipment may be assembled into a wide variety of possible configurations. This manual is intended to provide the basic information needed by the designer of such configurations. Details of the operation of particular interfaces or particular units are not included here, and may be found in the manuals relating to those interfaces and units.

2.2 OVERALL STRUCTURE

The central item in a 4080 system is the Central Processor Unit (CPU). The Basic Multiplexer Channel (BMC) used for the attachment of peripheral controllers, is an integral part of the C.P.U.

A simple 4080 configuration is shown in Figure 1. The CPU may be attached to several store units by individual store links. It is also attached to several peripheral controllers by the bus-connected Normal Interface. Most peripheral controllers are attached to one or more peripheral mechanisms.

If more peripheral throughput is needed, one or more Input/Output Processors (IOP) may be fitted. The standard IOP called the External Multiplexer Channel (EMC) produces an independent Normal Interface to which further peripheral controllers can be attached. An IOP must be connected to the processor unit, via the Command Interface, and to each store via individual store links. Figure 2 shows a system with an IOP.

2.3 IMPLEMENTATION

Processor

The 4080 processor and BMC form a rack-mounting unit, containing logic boards. An independent rack-mounted unit contains the power supply unit.

Several spare board positions (or 'slots') are provided. Logic boards plugged into appropriate slots have access to the store interface, or the Normal Interface.

Stores

Each store unit consists of a rack mounting unit with an independent rack mounted power supply unit.

A store link connects the store to the processor. The link consists of one board that plugs into the store unit, connected by a detachable cableform to one board which plugs into a slot in the processor unit. A store may accommodate up to four store links, the additional three being available for connection to IOP's.

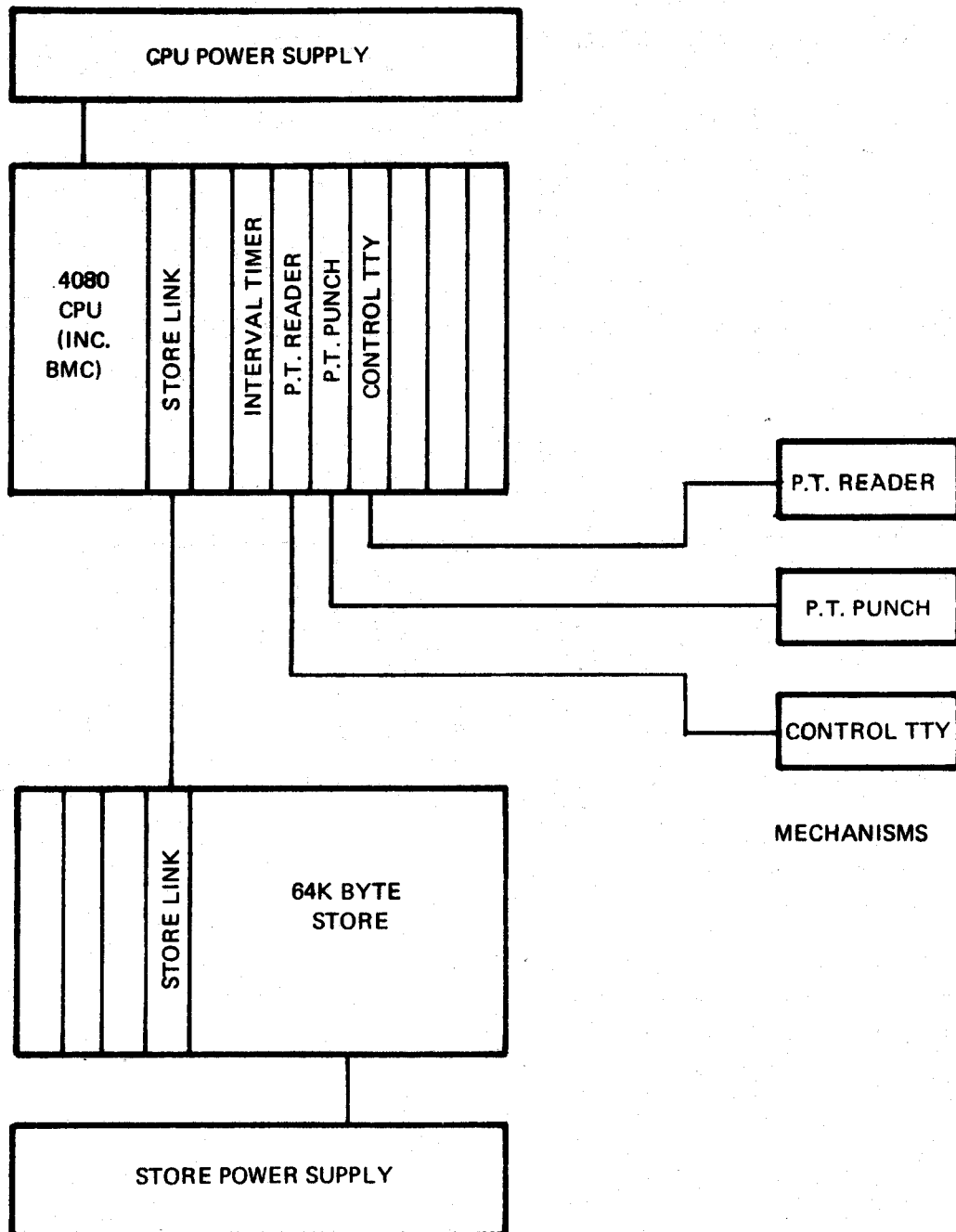
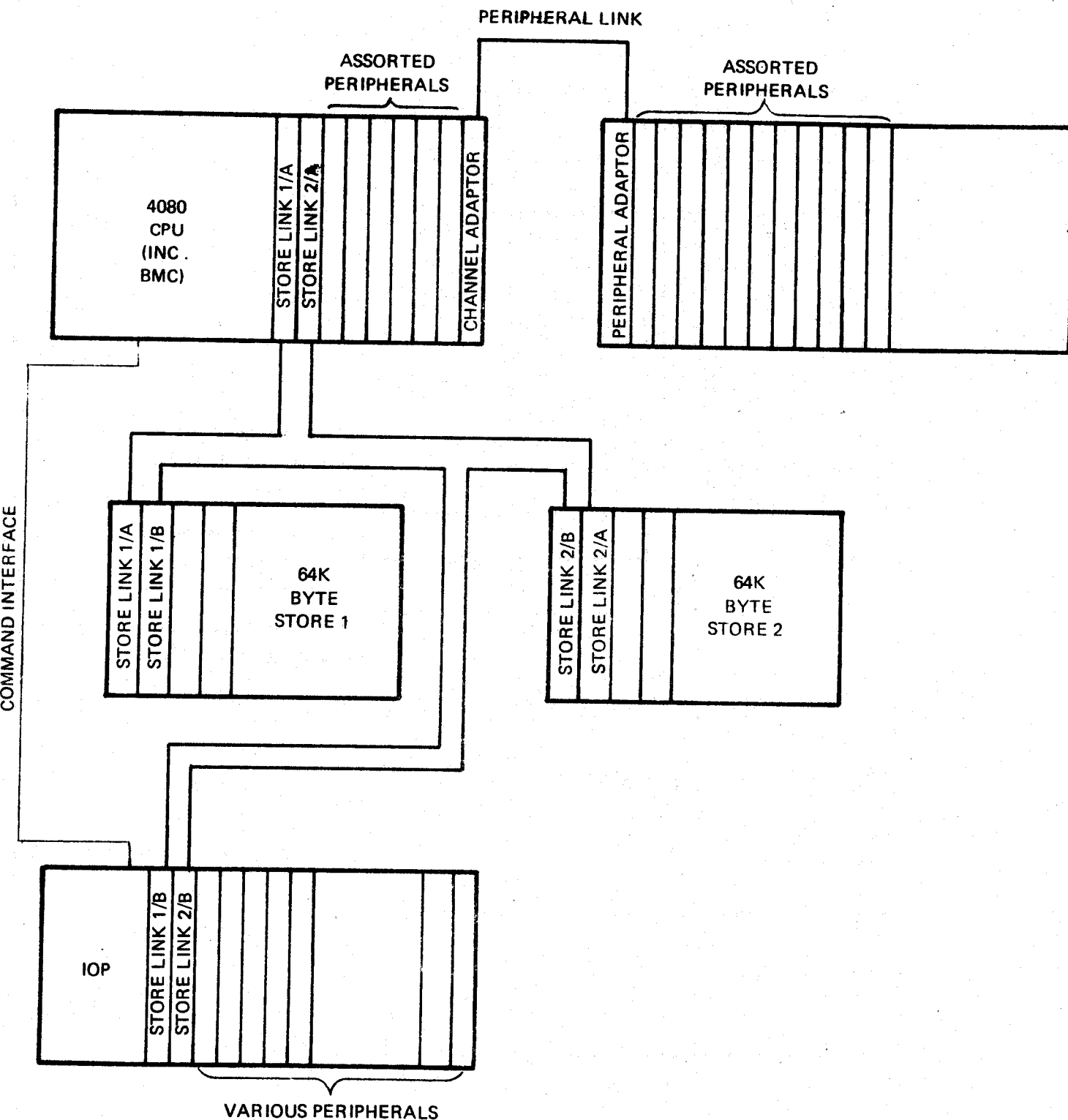


Figure 1: BASIC 4080 SYSTEM

SYSTEM DESCRIPTION



NOTE As drawn the IOP has priority over the CPU in Store 1, and vice versa in Store 2

Figure 2: BASIC 4080 SYSTEM

Peripheral Controllers

Each peripheral controller consists of one or more logic boards. These are connected by a detachable cableform to the associated peripheral mechanism, and obtain access to the Normal Interface by being plugged into a slot. This slot may be in the processor, or in the IOP if one is fitted. Since the number of slots so available is limited, additional slots are provided by Extension Units, described below.

Extension Units

An extension unit is used to provide additional slots for peripheral controllers. The extension unit is rack mounted, and has an integral power supply unit.

The extension unit must derive its Normal Interface directly or indirectly from the processor or IOP. A link occupies a dedicated board position in the extension unit, and is connected by a detachable cableform to a board which plugs into a slot where the interface is already available. These may be used in series i.e. plugged into another extension unit instead of directly to the processor or IOP. The use of links in series is generally to be avoided for peripherals with high data rates, since it inevitably increases cycle times and hence interface loading.

Switched Extension Units

An extension unit may be fitted with one or more additional links, so that it can be connected to more than one system, but only one such link can be operational at a time. An externally controlled switch selects which link shall be operational. Note that the additional links differ slightly from standard links, and each occupies a slot in the extension unit which would otherwise have been available for a peripheral controller board.

2.4 SUBJECTS FOR CONSIDERATION

The remainder of this manual gives more detail of a number of subjects effecting configuration. This subsection provides an overview, so that the interrelationship of the various parts may be seen.

Mains Distribution and Switching

Mains power must be provided to all power supply units, to logic racks for fans, and to peripheral mechanisms. The distribution and switching system is described in Installation and Standards manual.

Cabinet Space Allocation

The various rack mounting units must be assembled into cabinets, with blanking panels where necessary, and with regard to cabling and ergonomic considerations. Additionally, possible interactions between units must be taken into account. Details are given in the Installation and Standards manual.

Store Interconnection

The rules for store interconnection are straightforward. The processor unit must be linked to each store unit, and any IOP must be linked to the required store units. Address patches are set up on the store links to define the starting address of the store for the processor using the link. The C.P.U. must be capable of addressing all store units, IOP's need to access store 0 for control information. The store interconnection system is described in the Interface Manual.

Peripheral Devices

The arrangements for connecting peripherals to a 4080 system allow great flexibility, and allow large numbers of peripherals to be fitted. Inevitably, many interrelated aspects must be considered.

The major aspects are:

The allocation of peripheral controllers to slots in processors, and extension units, and the provision of links. Numbers of slots, power limitations and cable lengths must all be considered.

SYSTEM DESCRIPTION

The allocation of relative priorities to peripherals, and consequent setting of Ready numbers. This is related to the permissible interface throughput calculation, and to the allocation of slots.

The allocation of Way Numbers for peripheral selection.

Availability of standard or test software for peripherals, and for related requirements for other peripherals or for particular amounts of store.

These various aspects are considered in details as follows:

Slot allocation and d.c. power limitations-Section 5 of this manual.

Cable lengths and a.c. power limitations - Installation and Standards Manual.

Allocation of Way Numbers--Section 3 of this manual.

Allocation of priority to various peripherals, and hence Ready number allocation--Section 4 and Supplement 2 of this manual.

Input Output Processor

Data is to be found in the System section of the appropriate IOP manual. That document also provides information on the differences in interface loadings when a peripheral controller is connected to an IOP rather than to the BMC.

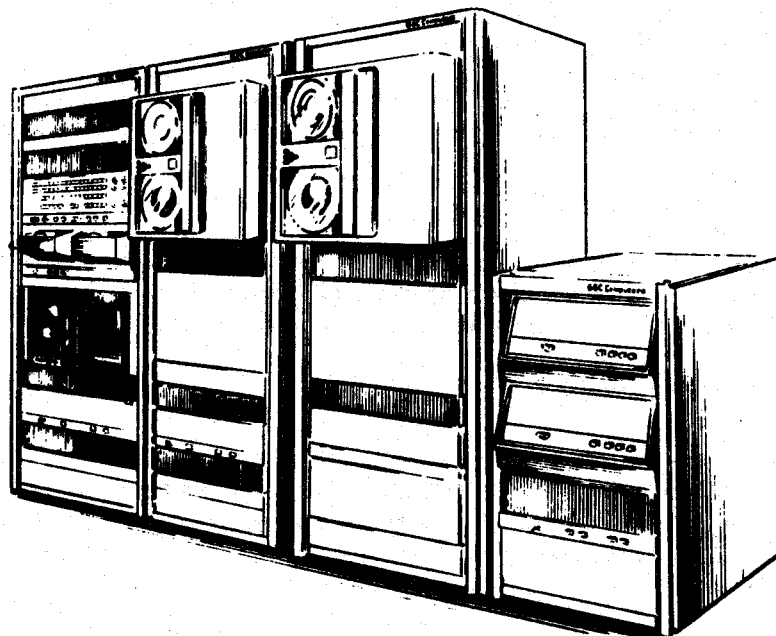


Figure 3: TYPICAL SYSTEM CONFIGURATION - PICTORIAL

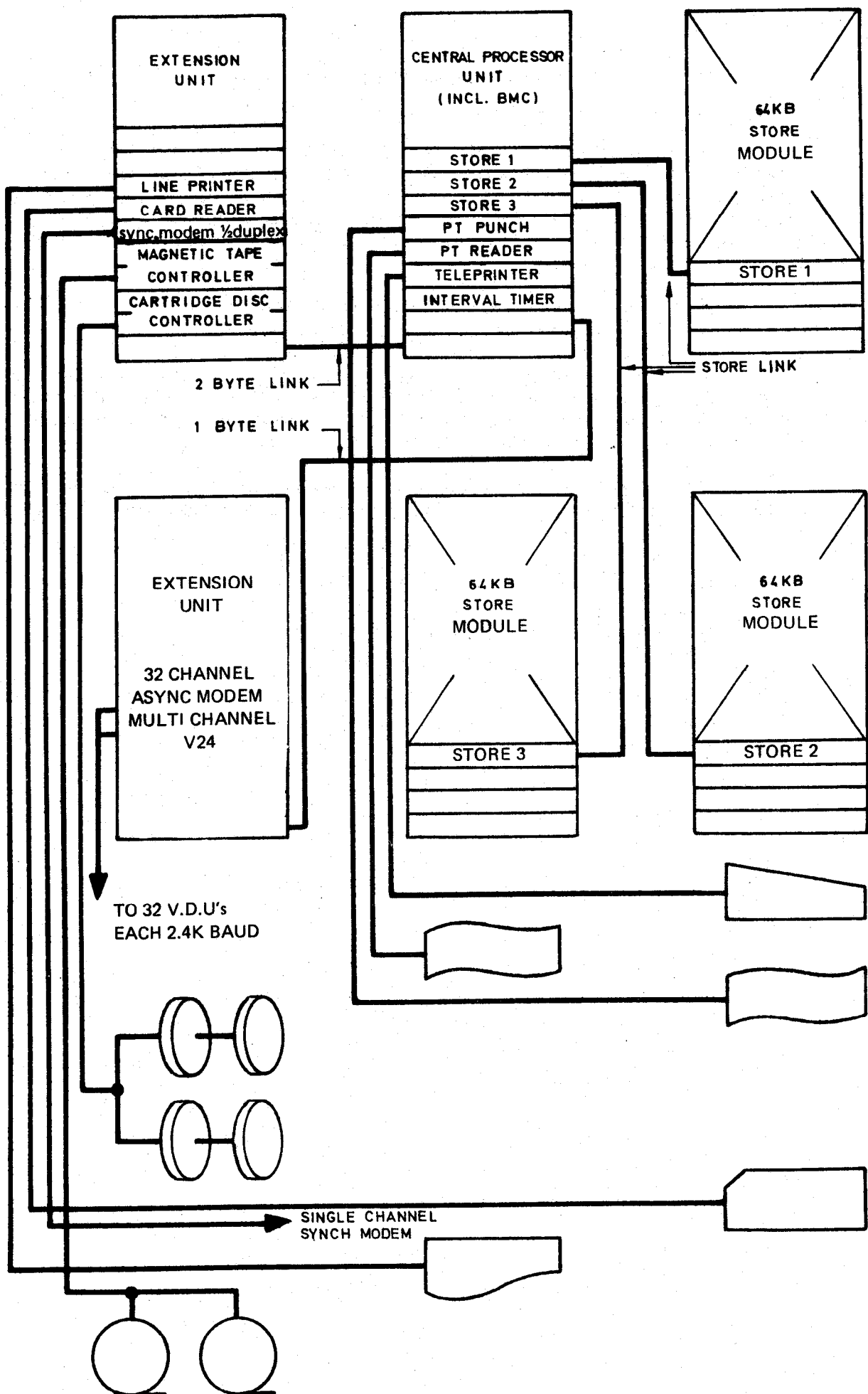


Figure 4: TYPICAL SYSTEM CONFIGURATION - BLOCK DIAGRAM

3

WAY NUMBERS AND READY NUMBERS

Peripheral controllers are connected to either the BMC or IOP via the Normal Interface (See **Interfaces Manual**). Each peripheral and each link to an extension unit occupying slots in a particular processor rack, must have a patched Ready number in the range 0 to 15, and a corresponding Ready line. These Ready numbers determine the allocation of interface cycles to the various peripherals and links, Ready 0 having the highest priority. The Ready number and line or link is set by means of a changeable patch panel on the board concerned.

The single Ready number available to a link is sub-multiplexed so that 8 or 16 Ready lines and Ready numbers are available on the secondary interface within the extension unit.

In addition to a Ready number, or numbers, a Controller is allocated one or more Way numbers in the range 0 to 255. The Way numbers provides a unique identification for the controller and enables the BMC to identify the area of core store associated with the controller. Way and Ready numbers are patched onto the controllers by means of small printed circuit boards plugged on to the controller board.

Certain Way numbers (see under) are allocated as standard to peripheral units, although in systems containing two or more identical peripherals only the first of each type is allocated the standard Way number.

PERIPHERAL	WAY NO.
Paper Tape Reader 500	0
Paper Tape Punch 110	1
Control Teleprinter or Thermal Printer	2
Line Printer	3
Interval Timer	7
Cartridge Disc	8 and 9
Magnetic Tape	10 and 11
H.P.T. Disc	12 and 13

4

NORMAL INTERFACE LOADING

4.1 SCOPE

This section explains Normal Interface loading and how transfer priority is accorded to the various peripherals in a system. A straightforward method of allocating Ready numbers, which is applicable without further verification, to lightly loaded systems, is described.

Supplement 2 provides a fuller method of analysing worst-case input/output conditions in which all the peripherals demand simultaneous transfers, to determine whether or not they can be serviced without performance degradation or transfer failure.

4.2 GENERAL CONSIDERATIONS

The Basic Multiplexer Channel (BMC) multiplexes and routes data transfers, via the Normal Interface, between store and any of up to 256 peripheral controllers (section 3). To enable this facility to be used without either loss of data or peripheral speed degradation the following rules must be obeyed,

- (a) The peak loading presented by such transfers must not exceed the capacity of the interface, and
- (b) peripheral priority allocation (Ready numbers) must be correctly made so that the transfer demands are satisfactorily interleaved and transfers serviced in time.

Once initiated, each autonomous transfer, whether in single or burst mode, occupies the interface for a period of time defined as the Hold Time (H). H depends on the design of each particular peripheral controller, the design of the channel controller and the length of any links over which the transfer passes.

A peripheral running at its nominal full rate demands transfers over the Normal Interface at intervals whose time duration is defined as its Repetition Time (R). Hence the loading, imposed by a peripheral, on the Normal Interface is given by

$$\text{LOAD} = \frac{H}{R} \times 100\%$$

The maximum safe load is limited to approximately 90% because of the interconnection between CPU and BMC requests for store cycles.

Most peripherals only maintain the level of interface load for a limited time, and must then wait for some mechanical operation. For example the lineprinter alternates between transfer phase and print phase. Thus the longer term mean loading may be less than that calculated above, and in certain configurations advantage can be taken of this fact. For the purposes of this section, however, the load is assumed to be continuous.

It should be noted, that to allow for safety margins in any loading calculations, all figures quoted in this manual are worst-case times which include allowances for design tolerances, deskewing etc. Furthermore the figures quoted for communications controllers are based on the shortest character setting in each case:

- (a) Asynchronous:- 5 - bit character with one start and one stop bit i.e. 7 units.
- (b) Synchronous:- 6 - bit character.

At a given data rate these settings give the highest loading factor.

The use of Extension Units and Links imposes restrictions on Ready number allocation, since the Normal Interface Link multiplexes the ready lines on its secondary interface to present a single ready line to the primary interface. A group of peripheral controllers housed in an Extension Unit share a single priority level with respect to other peripheral controllers or Extension Units connected to the primary interface. Thus, for example, if two Peripheral Link units, A and B are allocated Ready numbers 2 and 3 respectively all peripheral controllers on Link A have priority over those on Link B.

4.3 SIMPLE RULES FOR INTERFACE LOADING AND READY NUMBER ALLOCATION

Theoretical assessment of a generalised time-sharing mechanism indicates that, for load factors below 60%, the mechanism will always function correctly provided that time-slot allocations for each task are correctly ordered.

For a given GEC 4080 configuration, therefore, provided that the Normal Interface loading does not exceed 60%, the following simple procedure can be employed to allocate Ready numbers to the peripheral controllers. In the event that the loading factor exceeds 60% the interactive procedure given in Supplement 2 must be employed to verify correct operation of the interface or advice sought from GEC Computers Ltd.

(a) *Determination of Loading*

Any peripheral operating at full speed requires a specific percentage of the Normal Interface time to service its autonomous transfers. To determine whether or not a given group of peripherals can operate concurrently at full speed the percentage given in the LOAD column of Table 1 should be added. If this procedure indicates a total loading not exceeding 60%, Ready numbers allocated in the manner indicated in the following paragraphs ensure satisfactory operation.

(b) *Ready Number Allocation*

In 4080 configurations Ready numbers must be in the range 0 to 15. However each Ready number may be further subdivided when peripheral controllers are housed in an extension unit. The peripheral controller's Ready numbers are multiplexed onto one ready line on the link to the CPU. The link may be patched to any Ready number at the CPU.

For ease of reference Ready number notation 2/3 indicates a peripheral controller, with Ready number 3, housed in an Extension Unit which is connected, via a link, to the primary interface at Ready 2 (Table 2).

In principle any Ready number can be allocated to any device as long as the relative priority order is correct. If, as with Way numbers, two Ready numbers are required by a peripheral controller the mandatory rules in the description of the controller must be obeyed.

Configurations whose interface loading does not exceed 60% may have Ready numbers allocated directly in the order of Limiting Times as listed in Table 1. A full description of the term Limiting Times is provided in Supplement 2. Peripheral controllers with the lowest limiting time must be allocated the highest priority level and hence the lowest Ready number.

Table 2 provides a worked example of a typical configuration. The example has been checked using the procedure in Supplement 2 and the column headed ORDER refers to the results of priority allocation based on this procedure.

TABLE 1
PERCENTAGE LOADS AND LIMITING TIMES

PERIPHERAL	% LOAD	LIMITING TIME (μ s)
HPT Disc		
1:1 Interlace 16 bit N.I	69	34.0
1:2 Interlace 16 bit N.I	34	68.8
1:3 Interlace 16 bit N.I	23	103
16 bit N.I		
Cartridge Disc		
1:1 Interlace 16 bit N.I	38.2	65
1:2 Interlace 16 bit N.I	19.1	130
1:3 Interlace 16 bit N.I	12.7	195
Magnetic Tape System (30K)	11.9	130
Paper Tape Reader (500)	0.55	400
Line Printer (600/136)	1.9	880
Control Teleprinter (ASR 33)	0.008	4500
Card Reader	0.5	1200
Paper Tape Punch (110)	0.12	8000
Interval Timer (Interrupting every 1mS)	0.6	1000
Watch Dog and Interrupt Unit	0.0006	100,000
Modem Interfaces		
Asynchronous Half Duplex (7 unit character)		
600 baud	0.07	11600
1200 baud	0.13	5800
9600 baud	1.09	730
Synchronous Half Duplex (6 unit character)		
2400 baud	0.31	2500
4800 baud	0.62	1250
48K baud	6.2	125
Multichannel Asynchronous (7 unit character)		
16 channel 600 baud each channel	1.44	11600
32 channel 600 baud each channel	2.88	11600

SYSTEM DESCRIPTION

TABLE 2

TYPICAL SYSTEM CONFIGURATION (FIG. 4)

PERIPHERAL	CONNECTED TO CPU/EXTENSION UNIT	READY NO	ORDER
Paper Tape Punch (110)	CPU	5	4
Paper Tape Reader (500)	CPU	1	3
Teleprinter ASR33	CPU	4	4
Interval Timer	CPU	2	3
Line Printer (600)	EU	0/3	3
Card Reader (400)	EU	0/4	3
Sync Modem I/F (6 unit, 48K baud)	EU	0/1	2
Mag. Tape System	EU	0/2	2
Cartridge Disc (1:1 Interface)	EU	0/0	1
32 Async Multichannel I/F (7 unit 2.4K baud each)	EU	3/0	4

The Normal Interface loading of this configuration is approximately 71%. A configuration comprising any sub-set (or the whole) of that shown in Table 2 need not have the loading rules applied, providing that the Ready numbers allocated retain the relative priority sequence shown in Table 2, the actual value of the Ready number not being significant. If no specific reason exists for choosing particular number to form the sequence, the actual numbers given in the Ready No. column of Table 2 should be used for the sake of consistency.

5

SLOT ALLOCATION RULES

These rules must be obeyed when system configurations are specified. They arise from consideration of board position and power supply current. The mechanical requirements for the various peripheral controllers are:

Peripheral Controller	Slots Required	
Interval Timer	1	
Magnetic Tape	2	
Card Reader	1	
Cartridge Disc	2	
Head per Track Disc	3	
Paper Tape Reader (500)	1	
Paper Tape Punch (110)	1	
Control Teleprinter	1	
Line Printer	1	
Watchdog and Interrupt Unit	1	
Modem Interface	}	1
(Single Channel Synchronous or Asynchronous)		1
16 Channel Modem Interface		4
32 Channel Modem Interface		5

The 16 and 32 channel controllers must be housed in the EMC or Extension Unit.

Each store link occupies one slot in CPU or IOP as appropriate.

Each Normal Interface link occupies one slot in each of the two units linked.

5.1 CENTRAL PROCESSOR

The Central Processor Unit is slot, rather than power supply limited. A total of 9 slots are available for store links, peripheral links and peripheral controller boards.

5.2 EXTENSION UNIT

An Extension Unit is connected to a superior Normal Interface by a Peripheral link (Supplement 1) which requires one board position (slot) in the Extension unit. Each Extension Unit contains a further 13 slots. However, the total number of slots that may be used assuming averaged power consumption figures for peripheral controllers is limited by the maximum specified ambient temperature in which the unit has to operate. This relationship is shown as follows:

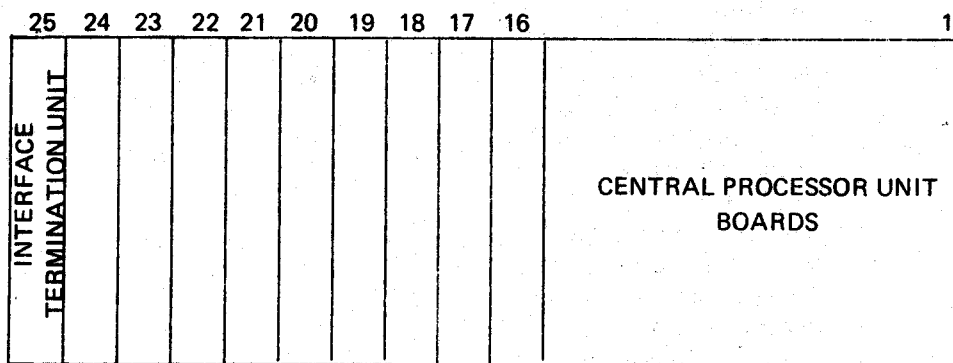
Temperature	Slots
55°C	8
50°C	9
45°C	10
40°C	11

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Thus any Extension Unit which is never subject to temperatures exceeding 40°C may contain a total of 11 boards of which 10 may be peripheral controllers.

Multi channel communication controllers take up to 50% greater power per board than average. Hence for power calculation purposes they consume 50% more slot power. In critical cases advice should be sought from G.E.C. Computers Ltd.

5.3 BOARD POSITIONING

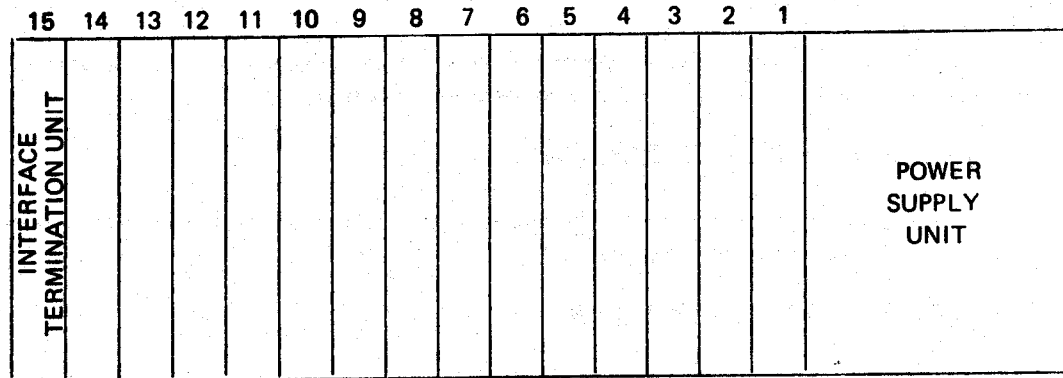


SLOT POSITIONS WITHIN CPU

Rules

- (a) Slot 25 is reserved for the Interface Termination Unit
- (b) Multiple board controllers, such as a disc controller, which require a link on EC2 can only be fitted into slots 21 to 24
- (c) Store interface link boards are fitted to slots 16 to 19.

- (d) Normal Interface peripheral controller boards and Normal Interface link boards are fitted to unused slots 16 to 24 starting with the lowest available number.



EXTENSION UNIT RACK

Rules

- (a) Slot 15 is reserved for the Interface Termination Unit
- (b) The Peripheral Adaptor board, that board connected to a superior Normal Interface, must occupy slot 1, and in a switched extension unit the second peripheral adaptor board must occupy slot 2.
- (c) Multiple board controllers may be fitted in any position. One board is connected to the Normal Interface, the other boards occupying the slots to the left.
- (d) Channel adaptor boards connected to further inferior Normal Interfaces, and peripheral controller boards should preferably be located starting from the lowest numbered and available slot.

6

OVERLOAD EFFECTS

This section of the manual summarises the effects, on peripheral equipment, of an overload on the Normal Interface i.e. if the Limiting Time (TL) for a peripheral is exceeded.

6.1 INTERVAL TIMER

An overload will result in loss of transfer and system action is liable to delay. Losses may be detected by use of the Interrupt Count Facility. Software recovery is necessary.

6.2 MAGNETIC TAPE CONTROLLER

A status report at the end of block will indicate transfer failure. Software recovery is necessary by Backspace followed by re-read or re-write as appropriate.

6.3 CARD READER CONTROLLER

A status report is given in the end of the read operation and the Reader stops. Manual re-insertion of the card is necessary.

6.4 CARTRIDGE AND HPT DISCS

Full sector buffering is provided in the controller, and if the filling or emptying of the buffer is momentarily slowed during a read or write operation on the disc, a complete disc revolution may be lost, depending on the state of the buffer. Recovery by re-reading or re-writing on the next revolution is automatically attempted by the controller. On a HPT disc unit a status indication is given.

6.5 PAPER TAPE READER (500) AND PUNCH (110)

An overload causes the transfer rate for both these units to slow down.

6.6 TELEPRINTER CONTROLLER (ASR33)

(a) *Read from Keyboard*

A transfer failure occurs, and a status report is given. Recovery action is by software and manual intervention.

(b) *Read from Paper Tape and Write to Printer/Punch*

Overload causes the transfer rate to slow down in both instances.

6.7 LINE PRINTER (300/136 and 600/136)

A delay in filling the Line Printer buffer causes an appropriate delay in the start of print-out and the printing rate is slowed.

6.8 WATCHDOG AND INTERRUPT UNIT

If the unit is in the CPU Primed mode it initiates an alarm unless the CPU performs a transfer to Watchdog every $1S \pm 10\%$. In the Interrupt mode the unit initiates an alarm unless the interrupt is acknowledged within 100ms.

Interrupts are latched and wait for service .Hence further interrupts on the same line which occur during the waiting period will be missed if the period is extended because of an overload.

6.9 MODEM INTERFACES

In the receive mode if transfer failure occurs, the recovery action depends on the system in question. In general recovery demands re-transmission of the message and hence is lengthy. In the transmit mode the transfer rate is slowed. Synchronous controllers insert a SYN character, which may represent a message failure depending upon the protocol in use. In all instances, a status report of such an occurrence is given at the end of the block transfer.

Supplement 1: LIST OF UNITS

1. 4080 Central Processor, Power Supply and Initial Program Load assembly
2. 4080 Core Store, Power Supply and Store Link
3. Extension Units and Normal Interface Links
4. Interval Timer
5. Watchdog and Interrupt Unit
6. Teleprinter
7. Reader 500
8. Punch 110
9. Cartridge Disc
10. Magnetic Tape 30 KHz
11. Line Printer 300/80, 300/136, 600/136
12. Single Channel Modem Interface Controller - Asynchronous
13. Single Channel Modem Interface Controller - Synchronous
14. Multichannel Modem Interface Controller - Asynchronous
15. Card Reader
16. Thermal Printer
17. Cyclic Redundancy Checking Unit
18. Teleprinter Compatible Display
19. Simple Graphics Display
20. Visual Display Terminal
21. External Multiplexer Channel
22. Dot Matrix Printer

4080 CENTRAL PROCESSOR, POWER SUPPLY AND INITIAL PROGRAM LOADER ASSEMBLY

The Central Processor Unit (CPU) is the fundamental unit of a GEC 4080 system. The CPU comprises three major electronic sub-assemblies, a Central Processor (CP) which provides the arithmetic and logic capability of the system, a Basic Multiplexer Channel (BMC) which provides the basic Input/Output capability of the system and a Control and Monitor Unit (CMU) by means of which both the CP and BMC are controlled, and which also provides wide ranging maintenance facilities.

The CP comprises eleven logic boards, the BMC three logic boards and the CMU a single logic board plus a panel of lamps and switches which forms the front panel of the CPU. The CPU provides positions for twenty-five logic boards of which fifteen are allocated for the CP, BMC and CMU, and one for an Interface highway termination board: the remaining nine board positions being available for units such as Store Interface Links or Peripheral Controllers.

The top third of the 12¼ ins. high CPU front panel is formed by a grill and filter through which air is drawn by cooling fans mounted on the rear face of the unit.

Initial Program Load (IPL) for a GEC 4080 system is achieved by loading a short program into store and subsequently acting upon the program. This program is held in Read Only Memories (ROMs) mounted on an Initial Program Logic Assembly, (IPLA) and its function will normally be to load systems software into store via a predefined peripheral device. The CPU provides for the fitting of two independent IPLA's, hence IPL can be performed from either of two peripheral devices. The IPLA's are located on the top edge connector of the Arithmetic board of the CP.

Three IPLA's are available; others may be added later -

IPLA Type 11

This provides for IPL from either a Paper Tape Reader 500 or the reader of a teleprinter

IPLA Type 12

This provides for IPL from a specially prepared file on a Magnetic Tape Handler.

IPLA Type 14

This provides IPL from a specially prepared file on a Head Per Track or Cartridge Disc Mechanism.

POWER SUPPLY

The Power Supply Unit (PSU) provides the DC power required by the CPU

The DC supplies provided by the PSU are sequenced, to ensure that system integrity is maintained, whilst the supply is switched on and off.

Power is supplied to the CPU by means of cables anchored at the processor and terminated at the PSU end by plugs and sockets. The PSU is cooled by fans mounted on its rear face; cooling air is drawn through a grill and filter on its front face and expelled at the rear.

OPERATIONAL CHARACTERISTICS

Formats

The CPU provides an extensive repertoire of instructions for arithmetic and logical operations on single bit, 8 bit (byte), 16 bit, and 32 bit data. Floating Point instructions are provided as standard, using 32 bit and 64 bit floating point number formats.

Performance

The CP is provided with extensive hardware support for multiprogrammed operation. In particular, store protection is provided by means of 4 hardware segment (Base and Range) registers whilst other aspects are handled by the hardware Nucleus.

The Nucleus provides a number of functions normally performed by a Software Executive.

These include:-

- Maintaining protection between programs
- Providing communications facilities between programs
- Short term scheduling of programs
- Providing fully protected Input/Output facilities
- Routing of interrupts to appropriate programs.

The communication feature is based on the use of messages passed between Co-routines; Semaphore claim and release operations are also provided to facilitate communication via shared data areas.

The CP has error handling capability, allowing the immediate action which may be necessary to prevent the effects of the error from propagating through the system. Upon error detection the Nucleus will form an error message and cause a reschedule operation to select an Owner or Error Process to run to deal with the error. The message contains an error code indicating the nature of the fault e.g. store parity failure, power failure, protection violation.

The CMU provides facilities for the Control of the CP and BMC, and facilities for the monitoring of registers and data highways within the CP and BMC for maintenance purposes. The front panel of the CMU provides:

- (a) Two rows of lamps on which register contents and data highways may be displayed. The information displayed is selected by 4 rotary switches.
- (b) One row of data switches. Data patterns set up on the switches may be written into hardware registers by operation of CMU controls, and may also be read, for engineering purposes, by programmed instructions.
- (c) Control switches and Indicator lamps. The control switches perform such functions as Reset/Run/Initial Program Load whilst the indicators display the CPU run state.

Interface

The BMC performs data transfers between I/O devices (such as peripherals and communications units) and main storage. Transfers of data are carried out via a standardised interface, called the Normal Interface; such transfers are carried out autonomously by the BMC in parallel with CP activity.

The Normal Interface provided by the BMC is a superset of that provided by the GEC 2050, differing only in the width of the Information highway : 16 bits are available with the 4080 BMC whilst the GEC 2050 provides only 8 bits of Information.

Summary of Operational Characteristics

CP :-	Instruction Length	16 bits
	Instruction Repertoire	180 Approx. including Floating Point
	Program Accessible Registers	8

Arithmetic and Logical Operations

Logical, 1 bit operands
arithmetic & Logical, 8 bit operands
arithmetic & logical, 16 bit operands
arithmetic & logical, 32 bit operands
Floating Point, 32 & 64 bit numbers

Main Store Capacity
Store Protection
Multiprogramming Hardware

32Kb - 256Kb
4 Hardware Segment Registers
Microprogram Nucleus providing
Protection, Communication, Scheduling
and Input/Output facilities.

BMC:-

Number of READY lines
Number of WAYS (= number of
simultaneous transfers)
Transfer types

16
256
Autonomous, 1 or 2 byte
Autonomous burst mode
Programmed, 2 byte

CMU:-

Control facilities
Monitor facilities
Number of points monitored
Store Test facilities

BMC test facilities

CPU test facilities

Include START, STOP, RESET, IPL
39 data lamps + 18 data switches
Approx. 1400 logic signals
Read or Write to store from CMU
switches and lamps
Initiate Autonomous transfer by
manual operation of CMU
Obey instruction from data switches,
take operand from data switches.
Micro step and Instruction step

Typical Operations Times (microseconds)

ADD			1.1
MULTIPLY	16 x 16	32	3.6
	16 x 32	64	5.85
DIVIDE	32 ÷ 16	32	20.35
BRANCH			1.35
SHIFT (N bits)			$2.3 + 0.5N$
BYTE STRING MANIPULATION (N bytes)			$1.55 + 2.35N$
REGISTER TO REGISTER			2.35
F.Pt. ADD	} 32 bit Operands	{	5.8
MULTIPLY			10.9
DIVIDE			19.4

The above are based upon a nominal store cycle of 550 nanosec..

The full set of Instruction times are given in the Performance Manual.

ELECTRICAL CHARACTERISTICS

D.C. Requirements

The separate PSU provides for the CPU

+5 volts	70 amps
+15 volts	1.5 amps
-15 volts	1.5 amps
-- 5 volts	5.0 amps

A.C. Requirements

Voltage – The nominal supply voltage to the Power Supply is preset to 200, 220v, 230v, 240v or 250v single phase by transformer tap selection.

Voltage variation $\pm 10\%$

Frequency – 48 – 66 Hz

Consumption – 1.0 KVA

Break Duration – Half cycle dropout.

In the event of a mains failure, the PSU down sequences the d.c. supplies in a prescribed order, and with sufficient time, for the processor to take the necessary action to avoid corruption of the program.

Power Control

Power is controlled via the ON/OFF switch located on the Central Processor control panel.

Protection

The Power Supply embodies protection against under voltage, over voltage and over current of the d.c. output supplies. Protection is also provide against over temperature of both the Power Supply and the Central Processor.

Main storage for a 4080 system is provided by modules of 2½D core store. The modules currently available are:-

Core Store, 32K Byte

This is a 19" rack mounting unit providing 32Kb of storage. Data may be written and read as 8 bit bytes or 16 bit halfwords. During a write operation parity bits are formed for each byte written, and during a read operation the parity of each byte read is checked. Parity failures are signalled to the Central Processor Unit (CPU), and are also indicated by a lamp on the front of the unit.

The unit includes a Store Access Director (SAD) which provides for the CPU and up to 3 Input/Output processors to be connected to the unit, via Store Interface Links.

Core Store, 64K Byte

This is similar to the 32K Store except that the unit provides 64 Kb of storage.

Core Store Expansion Unit, 32K Byte

This unit is provided to allow field expansion of the 32K byte Core Store, to provide a total of 64 Kb of core storage.

The Power Supply, Store

This 5¼" high 19" rack mounting unit provides DC power for one 32/64KB store module. The unit contains sequencing logic necessary for retaining store contents with mains failure.

Power is supplied to the store by means of cables anchored at the store end and terminated at the Power Supply end by plugs and sockets. The unit is force air cooled by fans mounted on its rear face; cooling air is drawn through a grill and filter on its front face and expelled at the rear.

The Store Link

It consists of a Store Link board which is plugged into a free board position in the processor, a Store Port board which is plugged into a free board position in the store module, and a pair of lightweight cables connecting the two boards. The maximum cable length is 10 ft.

OPERATIONAL CHARACTERISTICS

Formats

Store Width	16 bits + 2 parity
Module sizes	32 and 64 kilobytes

Performance

2½D ferrite core system having a nominal store cycle time of 550 nanoseconds.

A.C. Requirements

Voltage - The nominal supply voltage to the Power Supply is preset to 200, 220v, 230v, 240v or 250v single phase by transformer tap selection.

Voltage variation $\pm 10\%$

Frequency - 48 - 66 Hz

Consumption - 1.0 KVA

Break Duration - Half cycle dropout.

In the event of a mains failure, the PSU down sequences the d.c. supplies in a prescribed order, and with sufficient time, for the processor to take the necessary action to avoid corruption of the program.

Power Control

Power for a 4080 system is controlled via the ON/OFF switch located on the CPU front panel. A local ON/OFF switch is provided on the PSU rear panel.

Protection

The Power Supply embodies protection against under voltage, over voltage and over current of the d.c. output supplies. Protection is also provided against over temperature of both the Power Supply and the Core Store.

EXTENSION UNITS AND NORMAL INTERFACE LINKS

The extension unit is available to supplement the slots provided in the 4080 CPU for peripheral controllers. It may be used with any input/output processor which generates a normal interface.

Extension units are connected to the associated processor by means of a link. On 4080 systems this is usually either the single or two byte peripheral link. The link generates a secondary normal interface in the extension unit. The peripheral link is a multiplexing link, that is to say it multiplexes 16 Ready lines on the secondary normal interface, and uses one Ready line on the primary normal interface.

Extension Units

The number of peripheral controller and link boards that may be fitted is limited by the rated capacity of the power supply.

The use of switchable extension units and multiple links in multicomputer systems enables groups of peripheral controllers to be switched between the various processors. Switchable extension units may be controlled by either a local key operated rotary switch, or by a user supplied remote switching equipment, dependent on the system requirements.

Peripheral Links

A peripheral link consists of three sections

- (i) A channel adaptor board which plugs into the primary Normal Interface backplane
- (ii) A peripheral adaptor board which plugs into the secondary Normal Interface backplane
- (iii) One or two interconnecting cables. One cable carries the various control signals and the less significant byte of data. The second cable is only used for the 2 byte link, and carries the more significant byte of data.

There are two versions of peripheral adaptor board the standard and the type B. They differ in that the type B board does not contain any terminating resistors for the secondary Normal Interface.

Single links between a processor and an extension unit use a standard peripheral adaptor board. If there are multiple links between several processors and a switchable extension unit then one of the peripheral adaptor boards will be a Standard one, the remainder will be type B. In either case the interconnecting cables may be up to 30 metres long.

External Interface

The External Interface is provided to enable a user to connect his equipment to the Normal Interface without mounting it in a GEC Computers Ltd rack. This interface consists of a channel adaptor board and either one or two interconnecting cables as required.

Way and Ready Numbers

The links do not use a Way number, they have one Ready number on the primary Normal Interface.

INTERVAL TIMER

This unit is designed to generate interrupts to the Central Processor, the time interval between interrupts being controlled by software. The unit facilitates the maintenance by software of a Time of Day clock, as well as other timer facilities required for Real Time software.

The Timer comprises a single board of logic, which occupies a Normal Interface board position in the Central Processor shelf.

Formats

Time interval settings	250 μ sec min.
to	1.02375 sec max.
in	250 μ sec steps.

Performance

Long Term stability	less than 1 sec. drift in 24 hours.
---------------------	--

Interface

The Timer uses the 16 bit Normal Interface.

Way and Ready Numbers

The interval timer uses one Way and one Ready number.

WATCHDOG AND INTERRUPT UNIT

The Watchdog and Interrupt unit provides a means of monitoring the operation of the computer and also a means of routing signals from external equipment into the processor as interrupts. It is physically divided into two sections, a printed circuit logic board and a signal distribution unit.

Watchdog Unit

The Watchdog unit generates an alarm signal if it does not receive a program output transfer from the processor at a pre-specified time. The alarm signal may be used to activate a user supplied alarm.

Two main modes of operation are available. In one mode the Watchdog unit generates an alarm if it receives a program output transfer at any time except the period between 900 and 1100 milliseconds after the preceding program output transfer. In the second mode the Watchdog unit generates interrupts at one second intervals, and generates an alarm if a program output transfer is received at any time except for the 100 millisecond period after the interrupt has been generated.

The alarm state causes a pair of relay contacts to open. These contacts are available at the signal distribution unit.

External Interrupt Unit

The Interrupt Unit monitors the state of four pairs of lines, connected to it via the signal distribution unit. Whenever one of the lines changes state, in a pre-specified direction, then an interrupt is generated to the CPU.

The direction of change which causes the interrupt is pre-specified under program control. The unit contains logic to ignore contact bounce and signal oscillations on the line, after an interrupt has been initiated. This blanking period can be either 32 milliseconds (e.g. for relay generated signals) or 320 μ seconds (e.g. for logic driven signals) as determined by hardware patches.

Signal Distribution Unit

This small unit is generally mounted in the rear of the cabinet and contains five sockets with mating plugs which enable user supplied equipment to be connected to the alarm lines and interrupt signal lines.

Way and Ready Numbers

The Watchdog and Interrupt unit uses two consecutive Way Numbers. If both facilities are used then the even Way number applies to the Watchdog, and the odd Way number to the Interrupt unit. If only one facility is required then it can use any Way number. The unit uses one Ready number.

The Control Teleprinter provides a hard copy or paper tape output from the computer and permits messages to be input from either the keyboard or the integral paper tape reader.

The Control Teleprinter peripheral comprises a controller (which occupies one Normal Interface slot), a signal cable, a mains cable, and teleprinter mechanism.

Various versions of the mechanism are available i.e.

ASR33
DD390 (low noise version of ASR33)

All are complete with a floor stand.

The controller transfers data across the Normal Interface in 8 bit bytes. There are two modes of data transfer

(a) Binary Mode

The eight data bits are transferred directly to the teleprinter/controller interface on output (or vice-versa on input).

(b) Character Mode

The least significant seven bits are transferred as in Binary mode. The eighth bit is set to form overall even parity on output. On input the eighth bit is checked for even parity.

Performance

Keyboard Printer

Maximum speed	10 characters/sec (nominal)
Character set	ISO-7- UK (64 character subset)
Printer Column width	72 characters
Paper width	216 mm (8½ in.).

Paper tape Punch & Reader

Paper tape width	25.4 mm (1 in.)
Number of channels	8
Speed	10 characters/sec.

Interface

The 8 bit Normal Interface is used, data being transferred by autonomous input/output cycles. Burst mode is not used.

Way and Ready Numbers

The Teleprinter controller uses one Way and one Ready number.

PAPER TAPE READER 500

The Paper Tape Reader 500, is a paper tape input peripheral capable of reading at a maximum speed of 500 characters per second. The mechanism uses a dielectric reading principle.

The reader controller is built on one standard printed circuit board. This board plugs into any Normal Interface peripheral slot, and controls one reader mechanism.

The reader mechanism with tape dispenser is mounted in the rack mounting equipment which fits a standard 19" rack.

An interconnecting cable joins a connector on the controller board with a connector on the rack mounting equipment.

Formats

The reader controller transfers data in 8 bit bytes from the reader mechanism to the Normal Interface.

There are two modes of data transfer:

(a) **Binary Mode**

In this mode track 8 is transferred to the Normal Interface.

(b) **Character Mode**

In this mode track 8 is transferred to the Normal Interface as an 'O' and the controller checks even parity on the paper tape.

Performance

Reader Speed Nominal	500 characters/sec.
Tape	1" 8 hole Paper Tape or any Plastic Tape (not metallised) punched to BS.3880
Form	Coiled only.
Reader dispenser capacity	5" diameter coils.

Interface

The 8 bit Normal Interface is used, data being transferred by autonomous input cycles. Burst mode is not used.

Way and Ready Number

The Paper Tape Reader Controller uses one Way and one Ready number.

The Paper Tape Punch 110 is a paper tape output peripheral capable of punching at a maximum speed of 110 Characters per second.

The punch controller is built onto one standard printed circuit board. This board plugs into any Normal Interface peripheral slot and controls one punch mechanism.

The Paper Tape Punch mechanism is 19 inch rack mounting.

The inter-connecting cable joins an edge connector on the punch controller board with a connector on the punch mechanism.

OPERATIONAL CHARACTERISTICS

Formats

The punch controller transfers data in 8 bit bytes from the Normal Interface to the punch mechanism. There are two modes of data transfer:

- (a) Binary Mode - In this mode track 8 corresponds to the Normal Interface.
- (b) Character Mode - In this mode track 8 does not correspond to the Normal Interface, but is set to maintain even parity over each 8 bit byte on the paper tape.

Performance

Punch speed Nominal	110 Characters/sec.
Tape	1 inch 8 hole paper tape. Punched to BS. 3880
Tape Form	Coiled only, up to 1000 ft.
Punch dispenser	8½ inch dia. spools.

Interface

The 8 bit Normal Interface is used, data being transferred by autonomous output cycles. Burst mode is not used.

Way and Ready Numbers

The Paper Tape Punch Controller uses one Way and one Ready number.

CARTRIDGE DISC

The Cartridge Disc is a low cost backing store. The mechanism is of the moving head type using an exchangeable disc which can store approximately 2.5 Megabytes of usable data, i.e. 20 Megabits.

The mechanism may optionally include a fixed disc of the same data capacity and on the same spindle as the exchangeable cartridge disc.

The cartridge disc controller is built on two printed circuit boards which plug into adjacent Normal Interface peripheral slots and are connected by a link connector on the bottom of the boards. The controller is capable of driving up to two mechanisms (which may have a fixed and a cartridge disc each) and thus the maximum data capacity per controller is approximately 10 Megabytes, i.e. 80 Megabits.

The mechanisms are suitable for mounting in a 19 inch rack. Every mechanism is driven by a separate power supply which is mounted in a framework, also suitable for 19 inch rack mounting. This framework will house either one or two power supplies.

OPERATIONAL CHARACTERISTICS

Formats

Each disc has 204 tracks per surface at 100 tracks per inch.

Each track consists of 24 sectors, each containing the necessary preamble and post-amble, a hardware-checked header with its Cyclic Redundancy Code (CRC), 256 bytes of data and an associated 2 byte CRC.

Track seek operations may be carried out on 2 mechanisms at the same time. Data transfers however once initiated must be completed by the specified mechanism before another operation can be accepted by the controller. A write protect facility is provided on an individual track basis.

Performance

Average time to position heads	38 mS
Rotational Speed	2400 r.p.m. \pm 2%
Average latency	12.5 mS
Average transfer rate	246 Kbytes/second.

The controller may reduce this rate by a factor of 2, 3 or 4, as necessary to achieve an acceptable Normal Interface loading for the particular system.

Cartridge:- standard top loading (System 3) type - IBM 5440

Interface

Either the 8-bit or 16-bit Normal Interface may be used, data being transferred by autonomous cycles in Burst Mode, using burst of 8 bytes or 8 halfwords.

Way and Ready Numbers

The controller uses two Way numbers, a control Way number of the form $(2n)$, and a data Way number of the form $(2n+1)$ where $0 \leq n < 128$.

It uses one Ready number.

The Magnetic Tape 30 KHz provides a backing store for use on 4080 systems. The peripheral comprises a controller (occupying two Normal Interface slots), which is capable of driving up to four mechanisms in a bus configuration. The mechanisms are housed in standard (6') cabinets by means of special mounting metalwork. A cable connects the first handler to the controller, with an additional cable between each mechanism. The mechanisms will accept reels from 6" diameter to 10.5" diameter with standard IBM compatible centres.

OPERATIONAL CHARACTERISTICS

Data Formats

The transport operates at a standard tape speed of 37½ ips. The recording mode is NRZ1-at 800 bpi resulting in a transfer rate of 30K bytes/sec. The tape is recorded to standard 9 track format.

Interface

The 8 bit Normal Interface is used, data being transferred autonomously in bursts. Two way numbers (W1, W2) are used by the peripheral and data may be transferred in either of the following two modes:-

- (a) Direct: Data is transferred on Way W1, the store buffer being defined by Way Control Block W1.
- (b) Labelled: Data is transferred initially on Way W2. On expiry of the count in Way Control Block W2, the data stream is switched to Way W1 and the remaining data transferred. This mode is designed to enable the block address to be input separately from the main data.

The following control operations are implemented:-

Rewind, Rewind in Local, Erase, Write File Mark, and Backspace.

Way and Ready Numbers

As explained above the magnetic tape controller uses 2 Way numbers. W1 is of the form (2n) and W2 is of the form (2n+1), where $n \leq 0 < 128$.

The controller uses one Ready line.

A range of Line Printers provide a printing facility from 300 to 1250 lines per minute with column widths of 80 or 136 characters.

The unit comprises a mechanism which is free standing incorporating all necessary cooling and power supplied, a signal cable and a controller (occupying a Normal Interface slot)

OPERATIONAL CHARACTERISTICS

Operation

The Line Printer controller transfers data in 8 bit bytes from the Normal Interface to the Line-printer. The significance of this data depends on which mode of transfer is being used.

(a) **Output data mode**

In this mode data is printed with a layout which is solely determined by linefeed or carriage return characters in the data output string.

(b) **Paper feed and Output data.**

In this mode paper feed precedes the printing of data, with the movement of paper being determined by the vertical Format Unit, or can be a given number of lines up to 15. Linefeed and carriage return characters within the data strings are also obeyed.

Performance

Line printing speed	300, 600, 700 or 1250 lpm
Paper width	6 to 18 $\frac{1}{4}$ inches
Form length (fold to fold)	11 inch maximum for internal stacking
Vertical Format Unit	12 channels.

Interface

The 8 bit Normal Interface is used data being transferred by autonomous output cycles in bursts of four bytes.

Way and Ready Numbers

The Line Printer Controller uses one Way and one Ready number.

The unit is capable of directly controlling G.P.O. Datel 200 services using Modem No. 2 and G.P.O. Datel 600 services using Modem No. 1. In addition the controller is capable of operating the above services with automatic answering provided by G.P.O. Data Control Equipment No. 2A or, when limited to within the United Kingdom, by conforming to G.P.O. Specification TG 2316B.

Modemless working is possible where the device being controlled by the unit is local and telephone lines do not have to be used.

Three variants are available, one comprises a single standard board which will provide a half-duplex interface.

A second comprises a single standard board and associated interconnecting cable form to connect to a Post Office modem. This item will provide a half-duplex interface.

A third comprises two standard boards and associated interconnecting cable form to connect to a Post Office modem. This item will provide a full duplex interface.

OPERATIONAL CHARACTERISTICS

Format

The Modem Interface (Asynchronous) board controls the flow of data between the Normal Interface and modem lines in a half duplex mode. It converts data from a parallel word to serial data with the addition of start and stop bits (Transmit mode). In the receive mode the controller looks for a start bit and strobes in the following data bits. The controller can operate with 1 start and 1, 1½ or 2 stop bits.

Performance

Data transfer rates, typically vary between 50 and 9,600 bauds.

Number of data bits 5, 6, 7 or 8
(not including stop and start bits).

Interface

The unit is controlled by two interfaces

(a) The Normal Interface

The data is transferred in 8 bit bytes Autonomous input/output cycles. Where the transfer required is less than 8 bits, leading zeros are inserted

(b) Modem Interface

The signals are as specified by the CC ITT requirement V24 and are circuit numbers 102, 103, 104 108/2, 105, 125, 109, 116, 107, 106, 111.

Way and Ready Numbers

The single channel modem interface controller (asynchronous) uses one Way number and one Ready number.

SYNCHRONOUS MODEM INTERFACE

The unit is capable of directly controlling a Post Office Datel 2400 service using modem No. 7. In addition the unit is capable of operating the above service with automatic answering provided by Post Office Data Control Equipment No. 2A or, when limited to within the United Kingdom by conforming to Post Office Specification TG 2316B.

Modemless working is possible where the device being controlled by the unit is local, and telephone lines do not have to be used.

Three variants are available, one comprises a single standard board which will provide a half duplex interface.

A second comprises a single standard board, and associated interconnecting cable form to connect to a Post Office modem. This item will provide a full duplex interface.

A third comprises two standard boards and associated interconnecting cable form to connect to a Post Office modem. This item will provide a full duplex interface.

OPERATIONAL CHARACTERISTICS

Formats

The Modem Interface (Synchronous) board controls the flow of data in a half duplex mode between the Normal Interface and modem lines and converts data from 6 or 8 bit binary to serial, or vice-versa.

Character synchronism is achieved by generating on transmission two 6 or 8 bit sync characters, and on reception looking for two synchronising characters. The Syn. characters can be any 6 or 8 bit character.

Performance

Data transfer rates determined by clock from modem. Up to 50 Kbauds

Data transfer rates determined by internal clock 1 to 48Kbauds

Interfaces

The Modem Interface board is controlled by two interfaces:-

- (a) Normal Interface - Data is transferred by Normal Interface Autonomous input/output cycles.
- (b) Modem Interface - The signals are as specified by the CCITT requirement V24 and are circuit numbers 102 to 109, 111, 114 to 116 and 125.

Way and Ready Numbers

The Controller uses one Way number and one Ready number.

The unit is capable of directly controlling GPO Datel 200 services using Modem No. 2 and GPO Datel 600 services using Modem No. 1. In addition the controller is capable of operating the above services with automatic answering equipment provided by GPO. Data Control Equipment No. 2A or, when limited to within the United Kingdom, by conforming to GPO Specification TG 2316B.

Two versions of the unit are available. One provides up to 16 asynchronous half duplex V24 interfaces. The second provides for the capacity to be increased by a further 16 channels. The basic 16 channel unit consists of four logic boards, 3 cables and a protection unit. The expansion unit contains an additional board, a further 3 cables and a second protection unit.

The logic boards are usually housed in an extension unit. The protection units are separate 1½" 19" rack mounting units and contain the GPO approved protection units and 16 standard output connectors, one per half duplex channel. A full duplex channel requires two such connectors.

Cables are available for both half duplex and full duplex modem and V24 compatible peripherals.

OPERATIONAL CHARACTERISTICS

Format

A channel of the Multi-channel Asynchronous Modem Interface controls the flow of data between the Normal Interface and modem lines in a half-duplex mode. It converts data from a parallel word to serial data with the addition of start and stop bits (Transmit mode). In the receive mode the controller looks for a start bit and strobes in the following data bits. The controller can operate with 1 start and 1, 1½ or 2 stop bits.

Performance

Data Transfer rates, typically vary between 2400, 1200, 600, 300, 110 bauds.

Maximum data transfer rate is 2400 bauds for 32 channel unit, or 4800 baud for 16 channel unit.

Number of data bits 5, 6, 7 or 8, (not including stop and start bits).

Interface

The unit is controlled by two interfaces

(a) The Normal Interface

The data is transferred in 8 bit bytes by Autonomous input/output cycles. When the transfer required is less than 8 bits, then dummy bits are added.

(b) Modem Interface

The signals are as specified by the CCITT requirement V24 and are circuit numbers 102, 103, 104, 108/2, 105, 125, 109, 116, 107, 106, 111. Circuit 125 can be selected to operate a pulse release function.

Way and Ready Numbers

The Controller uses one Ready number, and up to 32 Way numbers, one for each channel. These Way numbers may start at any value below 225 and must run consecutively.

Two card readers are available which read standard 80 column, 12 row cards at a maximum rate of 400 or 600 cards per minute. Essential features are input card hopper, an output card stacker, a feed mechanism, an optical reading and timing station, control logic and an operator's control panel. The reader controller is built on one standard printed circuit board. This board plugs into any Normal Interface peripheral slot and controls one reader mechanism.

The card reader mechanisms is a free standing unit for desk or table top mounting.

OPERATIONAL CHARACTERISTICS

Interface

The reader controller transfers data in 8 bit bytes from the reader mechanism to the Normal Interface. Data is transferred by autonomous input cycles. Burst mode is not used.

Formats

Two modes of transfer are used:-

(a) **Uncoded mode**

The 12 rows in each column are read and transferred as two bytes.

The 12 rows are represented directly in two bytes as follows:-

Row	Byte	Bit
12	more significant (lower address)	0
11		1
0		2
1		3
2		4
3		5
4	less significant (higher address)	6
5		7
6		0
7		1
8		2
9		3

The convention 'no-punch = 0, punch = 1' is followed.

(b) Coded

The 12 rows are represented as one byte with the convention that no more than one of rows 1 to 7 is punched in one column.

Row	State	Bit	Value
0	no punch/punch	0	0/1
11	"	1	0/1
12	"	2	0/1
9	"	3	0/1
8	"	4	0/1
1-7	no punch	5-7	000
1	punch	5-7	001
2	"	5-7	010
3	"	5-7	011
4	"	5-7	100
5	"	5-7	101
6	"	5-7	110
7	"	5-7	111

This representation allows all 256 values that a byte may take to be uniquely represented as punched card columns. The convention used is one which is standard to all the commonly used card codes.

Character Representation

The representation of the standard character set (ISO-7-UK) on punched cards is in accordance with BS 4636 part 3 1971.

Performance

Reader Speed Nominal	400 cards per minute
Cards	80 column, 12 row cards to ANSI X3.11-1969 and USASI X3.21-1967.
Reader hopper and stacker capacity	500 cards, for 400 cards min: reader 1000 cards for 600 cards min: reader

NOTE: Cards may be loaded in the hopper and removed from the stacker during reading.

Way and Ready Numbers

The card ready controller uses one Way and one Ready number.

The Thermal Printer provides a hard copy output from the computer and permits messages to be input from the keyboard.

The Control Thermal Printer peripheral comprises a controller (which occupies one Normal Interface slot), signal cables, and a thermal printer mechanism modified by the addition of a local mains filter to the mains lead.

OPERATIONAL CHARACTERISTICS

Formats

The controller transfers data across the Normal Interface in 8 bit bytes. There are two modes of data transfer selectable by program.

(a) *Binary Mode*

The eight data bits are transferred by the controller from the mechanism to the Normal Interface (or vice-versa) and no changes or checks are performed.

(b) *Character Mode*

The least significant seven bits are transferred as in binary mode. The eighth bit is set to form overall even parity on output. On input the eighth bit is checked for even parity and set to zero before transfer over the Normal Interface.

Performance

The transmission speed is 30 characters/second nominal.

Printer Column width 80 characters.

Code and Character set

ASCII code with 64 print and key board characters.

NOTE: This differs from Teleprinter character set.

Interface

The 8 Bit Normal Interface is used, data being transferred by autonomous input/output cycles. Burst mode is not used.

Way and Ready Numbers

The printer controller uses one Way and one Ready number.

CYCLIC REDUNDANCY CHECKING UNIT

The Cyclic Redundancy Checking Unit is a self contained peripheral, data from computer store is received by the CRCU over the 8 bit Normal Interface.

The unit performs two functions:

- (a) To check data previously received over a communications link
- (b) To generate checking patterns to be transmitted over a communications link.

There is no limit to the length of data blocks that may be checked by the CRCU, blocks with odd numbers of bytes being permitted.

Various 16 bit and 12 bit checking polynomials may be selected by the use of a standard Way number patch and switching between 8 bit or 6 bit character working is by program control. Generation of checking patterns is commenced on receipt of the first byte of data and thus the final checking pattern is generated immediately after the end of the data block. This pattern is then transferred to main store.

The CRCU consists of one 484 board of standard TTL logic.

TELEPRINTER COMPATIBLE DISPLAY

The Teleprinter Compatible Display (TCD) has a V24 serial interface, and may be connected directly to a variant of the teleprinter interface board or an asynchronous modem interface controller. Alternatively it may be connected via modems with provision for full duplex operation using asynchronous modem interfaces.

OPERATIONAL CHARACTERISTICS

Display technique	625 CCIR T.V. standard (50Hz supply) 525 EIR T.V. standard (60Hz supply)
CRT size	12" diagonal
Phospor	P 4 white
Display area	9" wide, 5" high
Max. number of lines of characters	12
Max. number of characters per line.	80
Max. number of characters displayed and stored.	960
Character repertoire	63 displayed characters and symbols on 5 x 7 dot matrix. Space code does not alter displayed data.
Keyboard	The keyboard is provided with two-key rollover and the layout is similar to Teleprinter Layout.
Cursor form	Underline
Operator's cursor Control facility	Cursor home, LF, CR keys. Space bar moves cursor one position to the right, without altering displayed data.
Operator's erase facility	Clear screen key
Type of Interface	CCITT V24 asynchronous
Communications mode	Full duplex (echo back) only. (The half duplex position of the Full Duplex/Half Duplex switch is to enable data to be displayed directly from the keyboard, in the absence of a processor).
Data rates	Switch selectable choice of 2400 bauds and 1200 bauds. By alternative internal settings any two rates can be provided from the following range 110, 150, 300, 600, 900, 1200, 1800, 2400, 4800, 9600 bauds.
Data word format	1 start bit , 7 data bits, 1 parity bit, 2 stop bits for communication rates up to 300 bauds, or 1 stop bit for higher rates.
Parity	Switch selectable choice of even parity, odd parity or no parity.

The Simple Graphic display can present both graphic and alphanumeric information and has a V24 serial interface which may be connected directly to an asynchronous modem interface controller. Alternatively it may be connected via this interface over public telephone lines using modems.

The terminal consists of a display unit securely mounted on a pedestal. The display unit houses the screen, keyboard and operating controls. The pedestal contains the electronic units which operate the display and communicate with the computer.

OPERATIONAL CHARACTERISTICS

Modes of Operation

These are:

Alphanumeric
Graphic
Graphic Input

Alphanumeric Mode

Function:	Enter alphanumeric characters on Display from either keyboard or line.	
Format	35 rows of 74 characters (2590 characters total)	
Character Set	63 shapes + space	
Character Code	ASCII	
Character Size	height 2.7 mm (0.1 inch) width 1.8 mm (0.07 inch)	approx.
Character Generation	MOS ROM at 1200 characters/second 7 x 5 dot matrix	
Cursor Form	Flashing 8 x 5 dot matrix	

Graphic Mode

Function:	Enter vectors on S.G. Display from either keyboard or line.	
Vector definition	End co-ordinates (4 7-bit bytes for each co-ordinate)	
Addressable points	1024 x 1024	
Display area	1024 (x) x 780 (y)	
Vector writing time	2.6 ms.	

Graphic Input Mode

Function: Feed cross-hair cursor position to line.

Display identification Cross-hair cursor

Resolution 1024 (x) x 780 (y) points

Operator controls one thumbwheel per axis

Display

Display Medium 11 inch direct view bistable storage CRT.

Display area height 14.3 cm (5.6 inches)
width 19.1 cm (7.5 inches)

Usable Display Storage Time 1 hour

Interface

The following applies to the CCITT V24 communications interface.

Modes six, switched; covering Full and Half Duplex, local and line etc.

Transmission rates independently selectable for Send and Receive
110, 150, 300, 600, 1200, 2400, 4800, 9600 Baud asynchronous only.

The Visual Display Terminal (VDT) consists of a keyboard, and a cathode-ray tube display unit containing a MOS store, a power supply unit and a programmed interface controller.

The principle facilities provided by the VDT are as follows:

Edit

Full range of cursor movement controls

Cursor addressing from processor and identification of cursor position to the processor.

On line, off line, and block transmission modes.

Data compression technique. Characters which follow a delete code on the same line are not transmitted.

Program entry mode. In this mode, all control codes received from the processor or entered at the keyboard are displayed but not performed; but the two codes which cause the VDT to enter or leave this mode are not displayed.

Format mode. Protected data fields are not transmitted from the VDT when the VDT is in the the format mode.

Spaces on a line following a New Line code are not stored. More lines of data may be stored (the max. is 256 lines of 7 characters) than can be displayed at any one time. By scrolling up or down, either line-by-line, or page-by-page, any desired line may be brought into view.

A video output socket is provided for the connection of repeat display monitors.

OPERATIONAL CHARACTERISTICS

Display technique	525 EIA T.V. standard
CRT size	12" diagonal
Phosphor	P4 white
Display area	7½" wide x 6½" high approx.
Max. number of lines of characters	25
Max. number of characters per line	80
Capacity of store	2048 codes

Character repertoire

A total of 128 characters on a 5 x 7 dot matrix comprising:

- (a) 32 control code symbols, displayed in program entry mode only.
- (b) 63 ASCII punctuation, numerals and upper case characters.
- (c) 32 ASCII lower case characters (with descenders shifted down 2 line scans)
- (d) 1 Parity error symbol. The escape sequence control codes are displayed in the program entry mode only and appear as the equivalent ASCII characters displayed as black characters on a white background.

Display styles

- (a) White characters on a black background.
- (b) Black characters on a white background.
- (c) Blinking white characters on a black background.
- (d) Blinking black characters on a white background.

Form of cursor

Underline marker, blinking

Cursor movement controls

Up, down, left, right, home, carriage return, line feed, new line, tab, back tab.

Edit Functions

Page/Line edit, insert character, delete character, insert character delete line.

Erase Functions

Clear Store.

Erase to end of line. (In format mode erase to end of line. unprotected field).

Erase to end of store. (In format mode erase unprotected fields to end of store).

Scrolling

When a character is entered in the lower right hand corner of the screen, the display utilizing the SCROLL UP and SCROLL DOWN keys on the keyboard, the display will be scrolled either up or down a line at a time.

Utilization of the NEXT PAGE or PREVIOUS PAGE keys will cause the display to be scrolled either up or down 25 lines.

Data which disappears off the screen due to scrolling is not lost.

Type of interface

CCITT V24 asynchronous.

Communication Modes

Half duplex, or full duplex (echo back) switch selectable)

Data rates

110, 150, 300, 600, 1200, 2400, 4800, 9600 bauds
(switch selectable)

Data word format

Asynchronous mode

1 start bit, 7 data bits, 1 parity bit, 2 stop bits for data rate of 110 baud or 1 stop bit at higher rates.

Parity

Even.

Alternatively, a patch selection is available to omit the parity check and to generate a mark condition for the parity bit of all codes transmitted.

EXTERNAL MULTIPLEXER CHANNEL

The External Multiplexer Channel EMC is a high performance Input/Output processor which can communicate directly to core store i.e. allowing the EMC to function in parallel with 4080 CPU(s).

The EMC is an independent rack mounting type unit with mains filter, fans and a basic control panel. Cooling air is taken at the front and exhausted at the rear of the Unit.

The rack contains 2 logic boards, terminator board and up to 18 positions for store links and peripheral controllers. (maximum number of store links is 4).

INTERFACES

The EMC has 3 Interfaces:

Command Interface via which it is linked to the 4080 Central Processor and up to six other Input/Output processors.

Normal Interface this is a 16-bit interface which connects the standard peripheral devices to the EMC.

Store Interface which links the EMC to the store system.

PERFORMANCE

The EMC is capable of performing autonomous data transfers up to a maximum rate of 1.5×10^6 bytes/halfword per second. The actual maximum rate is dependent on peripheral and peripheral links design.

The number of peripheral controller boards housed is limited by power supply dissipation and ambient temperature as follows:

No. of Store Link Boards	No. of Peripheral Boards at			
	40°C	45°C	50°C	55°C
1	7	6	5	4
2	6	5	4	3
3	5	4	3	2
4	4	3	2	1

ELECTRICAL CHARACTERISTICS

Supply voltage	240v \pm 10%
Supply frequency	50Hz \pm 4%
Supply break duration	10 mS max.
Consumption	1.KVA approx.

DOT MATRIX PRINTER (100/80)

The Dot Matrix Printer operates at 100 characters per second over a maximum line width of 80 characters and 60 full lines per minute. This unit contains a line buffer and consists of a mechanism, a controller board and a signal cable.

The mechanism can handle paper to 9½ ins wide with ½ ins sprocket spacing and includes a two channel vertical format unit using 8 hole paper tape.

Formats

Printing is controlled by 8 bit (10 unit) asynchronous format transferred over a 24V serial interface from the Normal Interface, 7 bits only being significant. Software delays are necessary to prevent transmission during mechanism busy periods (see Performance).

Interfaces

The controller connects to the 8 bit or 16 bit logic level versions of the Normal Interface. The controller to mechanism interface is V24 serial, operating at 9600, 4800, 2400, 1200, 600, 300, 150 or 110 baud, with an 8 bit (10 unit) asynchronous format. The cable linking the controller to the printer has a maximum length of 500 ft. at a transmission rate of 9600 bauds.

PERFORMANCE

100 characters per second and 60 lines per minute.

The following commands to the mechanism cause it to go busy for the period indicated: These have to be allowed for in the supporting software.

Operation	Busy Periods
Line Feed	75 - 105 mS
Vertical Tab (1 inch)	300 - 310 mS
Form Feed (11 inches)	3 - 3 5 sec.
Delete	100 -400 µs
Select	100 -400 µs
Deselect	Until printer is selected
Print (CR or last character)	8.4 mS per character plus 75 -105 mS line feed. Printer is not busy during return time (270 mS max.).

A 250 mS delay occurs after a print command before printing commences if the main drive is not already running. Each print or paper movement command initiates a 9 second delay. If no other print or paper movement command is received during this 9 second interval the main drive motor is turned off.

Supplement 2: READY NUMBER ALLOCATION

The sequence in which simultaneous transfer demands are serviced on the Normal Interface is determined by Ready numbers allocated to the peripheral controllers, connected to the Normal Interface. The priority of the controllers is such that the unit with the lowest Ready number has highest priority.

Normally a peripheral controller operates as follows:-

- (a) Generates a Ready signal
- (b) Waits for time T_1 if necessary, for access to the interface whilst higher priority peripherals are serviced.
- (c) Occupies the interface for time T_2 to effect transfer.
- (d) Waits for time T_3 for peripheral to complete the requisite operation before generating the next Ready signal.

If T_4 is defined as the time between successive transfers from a given peripheral

$$\text{then } T_4 = T_1 + T_2 + T_3$$

Furthermore, if $T_3 \text{ min}$ is defined as the minimum time taken for the peripheral and controller to complete their house-keeping activities between the end of one transfer and the start of the next, T_1 may be extended until:-

$$T_1 \text{ max} = T_4 - T_2 - T_3 \text{ min}$$

It should be noted that for transfers in burst mode T_2 is the time taken to complete the burst.

$T_1 \text{ max}$ is called the patience of the unit whilst $T_1 \text{ max} + T_2$ is defined as the Limiting Time (TL).

If a transfer is not completed within time TL some form of degradation or transfer failure will occur. The effect of exceeding TL, for standard peripherals, is described in the System Description Manual section 6.

Many peripherals and their controllers do not directly conform to the simple pattern described, for example the Line Printer performs a series of burst transfers in rapid succession to fill its line buffer store and then relinquishes the interface for a long period whilst printing the line of text.

Some devices, for example Magnetic Tape Controllers, employ cyclic buffers as a protection against temporary delays on the interface, however, these devices impose strain on lower priority peripherals when recovering from a delay by imposing heavy demands on the interface whilst their buffers are refilled. A similarly heavy load is incurred when peripherals of this type start up. The Disc store controllers also function in this manner.

It should be noted that some relatively slow speed peripherals with fairly long patience, for example communications controllers in receive mode, can be the cause, if not serviced in time, of major system disrruption and of lengthy recovery procedures, whereas transfer failure with a high speed device with automatic hardware recovery such as a disc unit can be recovered much more rapidly (e.g. approximately 20mS for Disc units).

It is therefore clearly important to be able to determine whether, with a heavily loaded interface and with Ready numbers allocated in the order of Limiting Times (TL) of the devices, transfer interleaving can still occur satisfactorily in worst case conditions and with no degradation of peripheral performance.

It is of equal importance to know when this is not possible so as to allow for such exigencies in the design of the system.

Section 4 of the System Description Manual indicates that, provided the interface loading does not exceed 60%, allocation of Ready Numbers in order of Limiting Times ensures satisfactory interleaving under worst-case conditions.

Because of the interaction between CPU and BMC the maximum permissible load is about 90%.

For worst-case peak loading between 60% and the maximum, allocation of Ready numbers in order of device limiting times is still appropriate, but the checking procedures described in this Supplement must be employed in order to calculate whether delays can occur under worst-case conditions.

The Parameters listed are used in the checking calculation and/or appear as headings in the tables of worst-case figures (for standard peripherals) which are at the end of this Supplement.

- B:-** Burst duration (in μs)
- H:-** Hold time, may be greater than B if the peripheral normally operates with rapidly repeated bursts (in μs). Defined previously as T_2
- R:-** Repetition time. A peripheral operating at full speed uses H μs every R μs . Defined previously as T_4 .
- TL:-** Limiting Time. A peripheral must complete its H μs interface usage within TL μs . Defined previously as $T_{1 \max} + T_2$
- N:-** Number of bytes per burst.
- Rate:-** Mean number of bytes per second. For magnetic tape this assumes indefinitely long blocks.
- Load:-** The percentage utilisation of the Normal Interface. $\text{Load} = \frac{100 H}{R} \%$

It is assumed that the interface is initially quiescent and that a worst-case peak demand is imposed on the interface by all peripheral controllers setting their Ready lines true simultaneously. One of the peripherals, in practise that with highest priority, is serviced after a possible 2 μs delay if the CPU has been reading or loading a Way Control Block in store.

All controllers are assumed to set their Ready lines true again every R μs , the value of R varying from peripheral to peripheral. When a peripheral request is serviced, the peripheral occupies the Normal Interface for a period of H μs , where the value of H depends on the specific peripheral being considered. The initial condition, therefore, is that the sum of all the Hold Times of the peripherals, $(2 \mu s + \sum H_{all})$ is then pre-empted busy time when all peripherals demand simultaneous service.

It is clear that during such a time, $(2 \mu s + \sum H_{all})$ some peripherals, those with short repetition times R, will demand service more than once; thus pre-empting further hold times which must be added to $(2 \mu s + \sum H_{all})$ as the cycle continues, whilst other peripherals with long repetition times will not raise subsequent requests during the period $(2 \mu s + \sum H_{all})$. To determine whether, or not, satisfactory transfer interleaving will occur, it is necessary to perform an iterative calculation to determine when the cumulative time $(2 \mu s + \sum H_{all})$, also defined as the Continuous Busy Time CTB, becomes less than the time taken by an integral number (i) of demand cycles for each peripheral

Thus:- $2 \mu s + \sum H_{all} \leq \sum_i R_i$ of each peripheral where $i \geq 1$
 or $CTB \leq S_1, S_2, S_3, \text{ etc.}$

where $S_1 = \sum_1^i R_i$ for peripheral 1

$S_2 = \sum_1^i R_i$ for peripheral 2 etc.

At this point the iteration is halted since no peripheral is awaiting service, and thus it is possible to select those peripherals which need not have been serviced, by comparing individual TL times with the total CTB obtained. Peripherals whose TL exceeds CTB are allocated the lowest priorities and are eliminated from subsequent repetitions of the iteration.

The iteration is repeated as often as necessary to determine the behaviour of the remaining peripherals, eliminating one or more peripherals from the original complement at each iteration until only the highest priority peripheral or peripherals remain.

However, to allow for worst-case initial conditions, in the second and subsequent iterations, it must be assumed that the CPU just accessed the way control block and that the Normal Interface has just become occupied by one of the lower priority peripherals, eliminated at previous iterations, when the simultaneous initial demand for service occurs. Thus the initial value of CTB is set to $2\mu s$ plus the maximum B value from the lower priority peripherals eliminated in the previous iterations. It must be remembered that the use of Extension Units and Links generally increases the B and H times quoted in the tables by a factor of 20% for each Link over which a transfer passes.

If it is not possible to eliminate any peripheral after any iteration (i.e. when a value of CTB has been obtained which is less than $S_1 S_2 S_3$ etc. but which is not less than the TL for any remaining peripheral) this indicates that the peripherals concerned may not interleave transfers satisfactorily. In this case either the system should be reconsidered to reduce the interface loading or GEC Computers Ltd. should be consulted concerning further investigations possible.

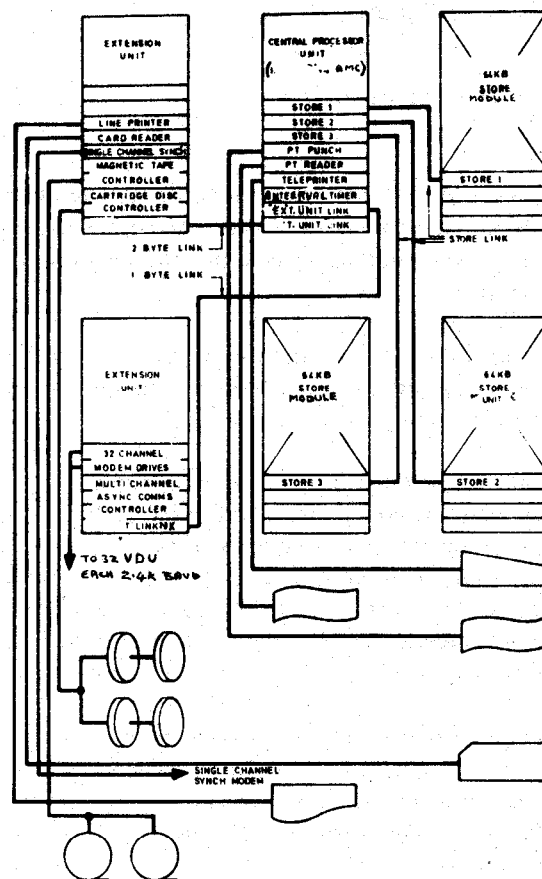
The following sequence summaries the iterative calculations described in the preceding paragraphs.

- (a) Set the value of CTB to $2\mu s$, for the first iteration, or to $2\mu s$ + the maximum B of any previously selected peripheral for subsequent iterations.
- (b) Set the initial S values of all remaining peripherals (i.e. those not yet selected) to zero.
- (c) Choose any remaining peripheral which has S equal to zero or $S < CTB$ and then add R to S to produce a new value of S and add H to CTB.
- (d) Repeat (c) until no peripheral has an S value less than CTB. Some peripherals may have to be operated on more than once before S is greater than CTB. The order in which the peripherals are dealt with is unimportant.

The final value of CTB obtained is compared with the Limiting Time (TL) of each remaining peripheral, and the peripherals whose TL exceeds CTB are now selected. These peripherals are assigned priorities higher than for any previously selected peripherals but lower than peripherals not selected. If two or more peripherals have values of TL greater than CTB, their relative priorities are unimportant, but for reasons of consistency these are still assigned in the order of Limiting Times if no other determining factors occur. The calculation is then repeated from (a) for those peripherals not yet selected.

Example of a Typical Ready Number Calculation

This example of a priority allocation algorithm is based on the configuration shown in figure 4 of the System Description Manual and, for convenience, reproduced overleaf.



The configuration is not particularly well designed since, for example, the disc controller is situated in an Extension Unit rather than in the CPU crate. Nevertheless the iterations show that interleaving will satisfactorily occur.

The communications interfaces are assumed to work with the worst-case character length, as given in the loading tables of the manual. The allocation of Ready Nos. within a priority group is arbitrary, although, for purposes of standardization, these are normally allocated in order of TL times.

Use of Calculation Sheet

- (a) Write name of Unit in Peripheral column
- (b) Tick + 20% column if Unit is housed in an Extension Unit
- (c) Complete TL, H and R columns from data in Table 1 ensuring that H is increased by 20% for each link where appropriate
- (d) Add H values to produce ΣH all and an additional $2\mu s$ for Nucleus instruction allowance (BMC locked-out); at second and subsequent iterations add in the maximum H of any previously selected peripherals, to arrive at Total Initial CTB
- (e) Transfer the value obtained for CTB to the first previous CTB position (under first S value column). Compare CTB with R values, and if $CTB >$ than any R value, insert 2R in first S value column for each peripheral. Add the H value for each peripheral, whose R value was $<$ than CTB, to CTB. Continue this procedure using values 3R, 4R etc for S as well as adding H to previous CTB until all S values $>$ CTB

Note: Tick the first column if the controller is connected via a link and adjust H by + 20%

JOB :-	CONFIGURATION EXAMPLE IN SYSTEM MANUAL
ITERATION NO. :-	1
SHEET NO. :-	1

+ 20%	PERIPHERAL	T _L	H _M	R _S	CURRENT S VALUES (Σ R _i for each peripheral) i=1								Iteration stops when all S values > CTB Selected peripherals have TL > CTB					
	P.T. PUNCH	8000	11	9180									↑					
	P.T. READER	100	11	2000														
	TELEPRINTER	4500	8	100,000									↑					
	INTERNAL TIMER	1000	6	1000					2000					↑	INDICATES PERIPHERALS SELECTED AS LOWEST PRIORITY SINCE THEIR TL > CTB.			
	LINE PRINTER (600)	880	18	880					1760									
*	CARD READER (100)	1200	12	1900														
*	SYNCHRONOUS I/F (18K Baud)	125	10	125	250	625	875	1125	1250	1375		1500						
*	MAG. TAPE	130	19	130	260	650	910	1170	1300	1300	1430							
*	C.DISC (1:1)	65	29	65	130	650	910	1105	1235	1300	1365	1430						
*	32 CH. ASYNCH. MODEM I/F (2.4K Baud)	2900	365	2900									↑					
Σ Hail Add		489	2	-		↑	↑	↑	6	↑			↑	AT THESE STAGES MULTIPLES OF H AND R HAVE BEEN ADDED TO CTB AND S RESPECTIVELY. THESE MULTIPLES ARE CHOSEN TO MAKE S GREATER THAN PREVIOUS CTB.				
Add max H of selected peripheral		-	-	-					18									
TOTAL INITIAL CTB		491				10	3x10=30	2x10=20	2x10=20	10	10							
						19	3x19=57	2x19=38	2x19=38	19	0	19	10					
						29	8x29=232	4x29=116	3x29=87	2x29=58	29	29	29					
ADD H OF REPEATED CYCLES PREVIOUS CTB						491	549	868	1012	1211	1298	1337	1385					
CURRENT CTB						549	868	1012	1211	1298	1337	1385	1424					

H 3155

Note: Tick the first column if the controller is connected via a link and adjust H by + 20%.

JOB :-	
ITERATION NO. :-	2
SHEET NO. :-	1

[illegible]

N 3155

Note: Tick the first column if the controller is connected via a link and adjust H by + 20%

JOB :-	
ITERATION NO. :-	3
SHEET NO. :-	1

[illegible]

H 3155

- (f) At this point select as the lowest priority those peripherals whose TL is $>$ CTB achieved
- (g) Repeat the procedure steps (a) to (f) for the remaining peripherals whose TL $<$ CTB with the exception that Total Initial CTB must include the maximum H value of the selected peripherals.

The results of this worked example are summarised in the following table (see 4.3).

PERIPHERAL	CPU/EU	PRIORITY GROUP	READY NO.
Tape Punch	CPU	4	5
Tape Reader	CPU	3	1
Control Teleprinter (ASR33)	CPU	4	4
Interval Timer	CPU	3	2
Line Printer (600)	EU	3	0/3
Card Reader (400)	EU	3	0/4
Sync ½ duplex Modem I/F (48K Baud)	EU	2	0/1
Magnetic Tape System	EU	2	0/2
Cartridge disc	EU	1	0/0
32 ch. Modem I/F ½ duplex (2.4K Baud)	EU	4	3/0

It may be noted that the peripherals in group 3 are partly located in the CPU and partly in the Extension Unit, their priorities are allocated such that the grouping is correct but because of the location of the peripherals their individual priorities within the group are not in order of their TL values.

Table 1: PERIPHERAL LOADING SUMMARY

ITEM	UNIT	Rate Bytes /sec.	N	Load (%)	TL (μ s)	B (μ s)	H (μ s)	R (μ s)	Width (bytes)	NOTES
1	Interval Timer	N/A	1	0.6	1000	6	6	1000	2	Assumes interrupts at 1 ms intervals.
2	Magnetic Tape Controller	30K	4	11.9	130	15.8	15.8	130	1	
3	Card Reader Controller	533	1	0.5	1200	10	10	1.9K	1	
4	Cartridge Disc Controller									
	1:1 Interface	246K	8	38.2	65	23.8	23.8	65	2	
	1:2 Interface	123K	8	19.1	130	23.8	23.8	130	2	
	1:3 Interface	82K	8	12.7	195	23.8	23.8	195	2	
5	HPT Disc Controller									
	1:1 Interface	410K	8	69	34.4	23.8	23.8	34.4	2	
	1:2 Interface	205K	8	34	68.8	23.8	23.8	68.8	2	
	1:3 Interface	137K	8	23	103	23.8	23.8	103	2	
6	Paper Tape Reader (500)	500	1	0.55	400	10.5	10.5	2K	1	
7	Paper Tape Punch (110)	110	1	0.12	8000	10.7	10.7	9.1K	1	
8	Teleprinter Controller (ASR Type 33)	10	1	0.008	4500	8.0	8.0	100K	1	
9	Lineprinter 600/136	1.36K	4	1.9	880	17.4	17.4	880	1	
10	Watchdog & Interrupt unit	N/A	1	0.0006	100K	5.7	5.7	1M	1	

Table 1: PERIPHERAL LOADING SUMMARY

ITEM	UNIT	Rate bytes /sec.	N	Load (%)	TL (μ s)	B (μ s)	H (μ s)	R (μ s)	Width (bytes)	NOTES
11	V24 Modem Interface Units									For all Modem interface controllers the value of TL may vary depending on the unit at the far end of the link. Full duplex links use a pair of interface units which are treated independently for loading calculations.
11A	Asynchronous Half Duplex 7 unit data									
	e.g. 600 baud	86	1	0.07	11.6K	7.7	7.7	11.6K	1	
	1200 baud	172	1	0.13	5.8K	7.7	7.7	5.8K	1	
	2400 baud	343	1	0.27	2.9K	7.7	7.7	2.9K	1	
	9600 baud	1371	1	1.09	730	7.7	7.7	730	1	
11B	Synchronous Half Duplex 6 unit									Full duplex links use a pair of interface units which are treated independently for loading calculations.
	e.g. 2.4K baud	400	1	0.31	2500	7.7	7.7	2.5K	1	
	4.8K baud	800	1	0.62	1250	7.7	7.7	1.25K	1	
	48K baud	8K	1	6.2	125	7.7	7.7	125	1	
11C	Multi-channel Asynchronous Half Duplex Modem Interface V24 Comms. Controller 7 unit data mounted in an extension unit.									In this case there is only one Ready line. Hence the effect of several channels is to retain TL, H and R at constant values, and to vary Load and B according to the number of channels in use.
	600 baud	86	1	0.09	11.6K	9.5	9.5	11.6K	1	
	1200 baud	172	1	0.18	5.8K	9.5	9.5	5.8K	1	
	2400 baud	343	1	0.37	2.9K	9.5	9.5	2.9K	1	
	e.g. 32 channel at 2.4K baud	11K	1	11.5	2.9K	10.5	304	2.9K		
				TOTAL						

Table 1: PERIPHERAL LOADING SUMMARY

ITEM	UNIT	Rate bytes /sec.	N	Load (%)	TL (μ s)	B (μ s)	H (μ s)	R (μ s)	Width (bytes)	NOTES
12	Thermal Printer used as a TTY	30	1	.02	33.3K	8.0	8.0	33.3K	1	
13	V.D.U. used as TTY	120	1	.19	8.33K	8.0	8.0	8.33K	1	