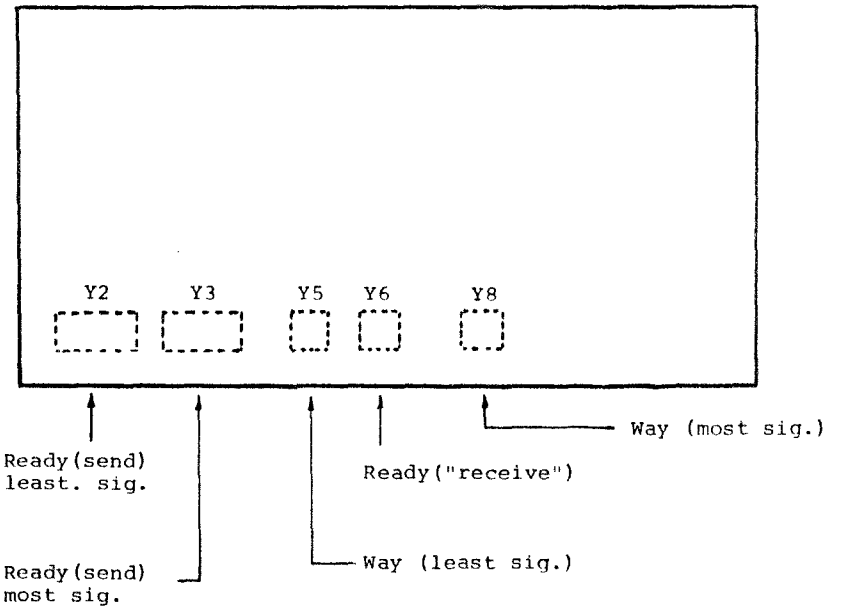
WAY and READY PATCHING

Way and Ready patching when applicable to P.C.B.'s, is always held between Court Areas Y2 to Y8.
In most cases boards will contain Way and Ready patching.

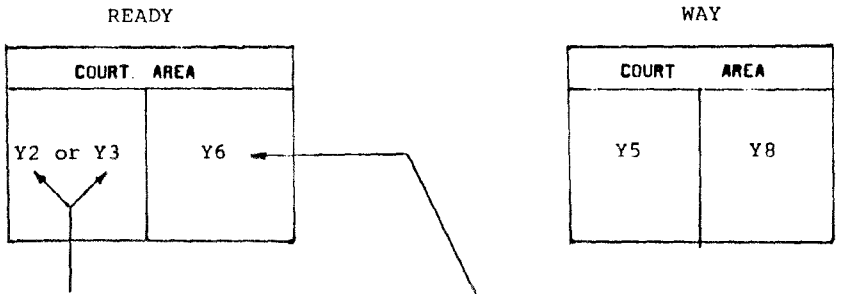
For the purpose of this excercise we are not concerned with the function of the Ways and Readies but only with the mechanics of patching the boards and interpretation of the information on the sheets provided.

A typical board is shown below.



Information on board sheets takes the form:

READY EXAMPLE



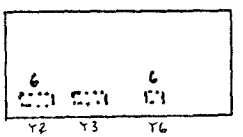
This means READY patching is req'd in court areas Y2 or Y3 depending on the ready value.

ie. If Ready is less than 8 put patch on Y2
Ready will = Patch No.
If Ready greater than 7 put patch on Y3.
Ready will = Patch No.+ 8

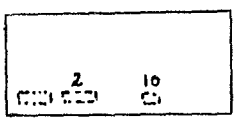
Ready patch placed on Y6 MUST be of equal value to to the Ready set up on Y2 or Y3.(see example)

examples

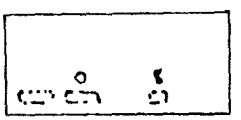
If Y2 patch is = 6 then
Y6 patch must = 6
} Says Ready 6



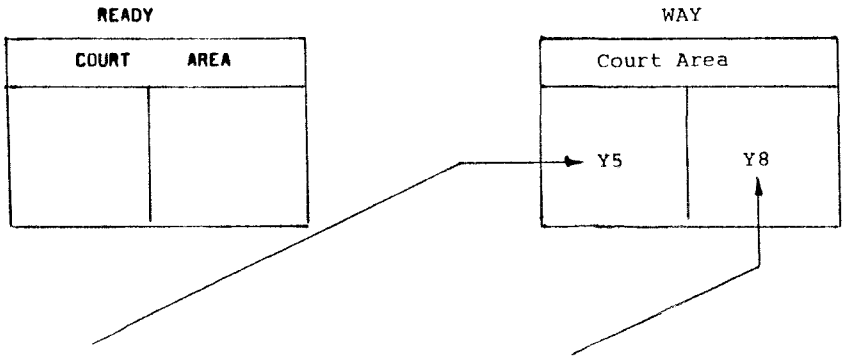
If Y3 patch is = 2 then
Y6 patch must = 10
(2 + 8)
} Says Ready 10



If Y3 patch is = 0 then
Y6 patch must = 8
(0 + 8)
} Says Ready 8



WAY EXAMPLE



WAY patch least sig. req'd in this court area.

May be from 0 to 15

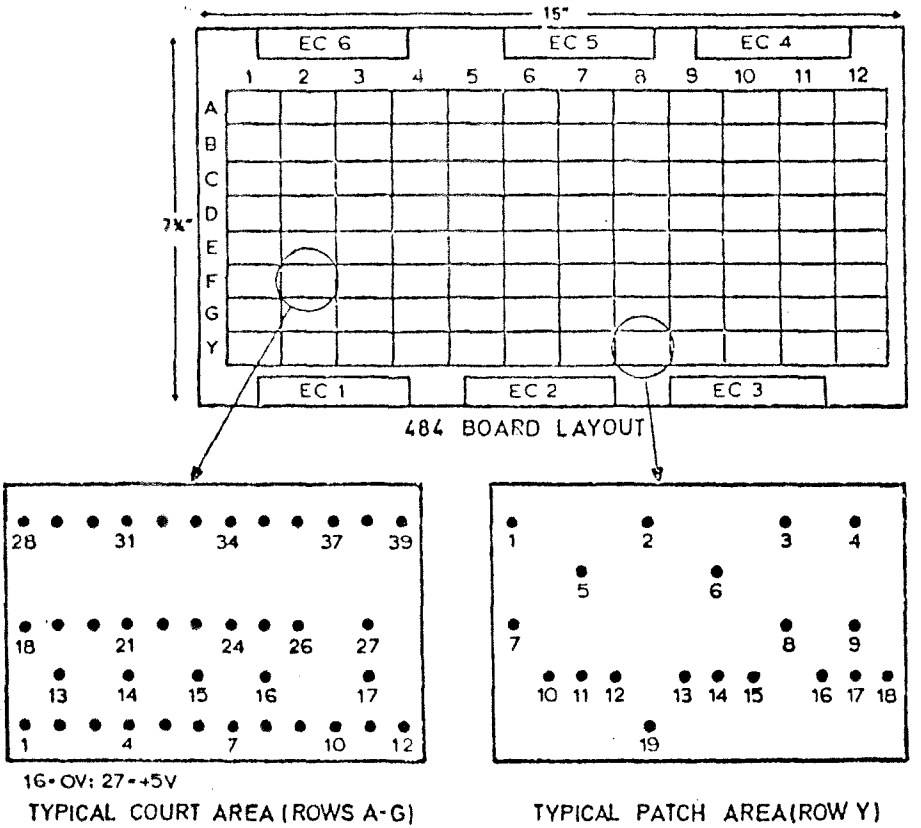
ie. Patch 7 = Way 7

WAY patch req'd here for most sig.
If Way No. is less than 16 put Patch 0 on Y8.

If greater than 15 then divide by 16, round down to nearest whole number, place that on Y8 and remainder on Y5.

examples

WAY NUMBER	Y5	Y8
2	2	0
15	15	0
16	0	1
33	1	2



COMPONENT SIDE VIEW

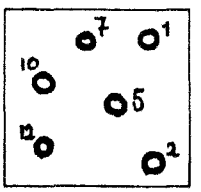
Figure 8: STANDARD LOGIC BOARD

WAY AND READY PATCH DETAILS

There are 16 different way (WRP) patches and 8 different ready(RLP) patches.

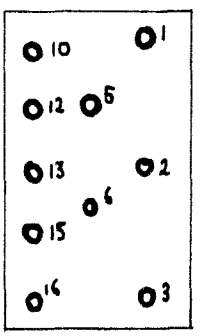
WRP	LINK TOGETHER	LINK TOGETHER
0	1,7,10,5and 2	---
1	1 and 12	7,10,5 and 2
2	5,1,7 and 10	2 and 12
3	1,2 and 12	7,10 and 5
4	2,5,1 and 10	7 and 12
5	1,7 and 12	5,2 and 10
6	5,1 and 10	2,12 and 7
7	7,1,2 and 12	5 and 10
8	2,1,7 and 10	5 and 12
9	1,5 and 12	7,10 and 2
10	1,7 and 10	2,5 and 12
11	1,5,2 and 12	7 and 10
12	2,1 and 10	5,12 and 7
13	7,1,5 and 12	2 and 10
14	1 and 10	7,12,5 and 2
15	7,1,5,2 and 12	---

WRP PATCH ONLY
Pin 10 = 0 volts
Pin 12 = 5 volts



WRP PATCH

RLP	LINK TOGETHER	LINK TOGETHER
00	1 and 3	2 and 5
1	2 and 6	5 and 3
2	2 and 10	3 and 6
3	2 and 12	3 and 10
4	3 and 12	2 and 13
5	2 and 15	3 and 13
6	2 and 16	3 and 15
7	3 and 16	---



RLP PATCH